	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 2003114798 A	☐	DATA PROCESSING METHOD FOR SUPERSCALAR PROCESSING SYSTEM	
2	JP 2003067184 A	☒	CHECKPOINTING OF SUPERSCALAR OUT-OF-ORDER PROCESSOR FOR ERROR RECOVERY	
3	JP 2002318687 A	☒	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
4	JP 2002007118 A	☒	VLIW PROCESSOR	
5	JP 2002318687 A	☒	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
6	JP 2002007118 A	☒	VLIW PROCESSOR	
7	JP 2001243067 A	☒	SUPER SCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
8	JP 2001229023 A	☒	SUPERSCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
9	JP 2001216157 A	☒	INSTRUCTION RETRIEVAL AND PORT ALLOCATION (FIAP) CIRCUIT AND ITS METHOD	
10	JP 2001092657 A	☒	CENTRAL ARITHMETIC UNIT AND COMPILE METHOD AND RECORDING MEDIUM RECORDING COMPILE PROGRAM	
11	JP 2000339163 A	☒	SUPER SCALAR MICROPROCESSOR, ITS PROCESSOR SYSTEM, DATA PROCESSING METHOD IN THE SAME AND COMPUTER SYSTEM PROVIDED WITH PROCESSOR	
12	JP 2000339162 A	☒	SUPER SCALAR MICRO PROCESSOR	
13	JP 2002095289 A	☒	LARGE COUPLING WIDE BAND OR NARROW BAND EXCHANGE	
14	JP 2002076351 A	☒	PROCESSOR HAVING LOCAL INSTRUCTION LOOPING	
15	JP 2001048484 A	☒	REGISTER NAME CHANGE SYSTEM	
16	JP 2000039996 A	☒	SUPERSCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
17	JP 2000029698 A	☒	SUPER SCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	

	Document ID	U	Title	Current OR
18	JP 2000029697 A	☒	SUPER SCALAR PROCESSOR, DATA PROCESSING METHOD AND COMPUTER SYSTEM	
19	JP 4113451 21 A	☒	INSTRUCTION EXTRACTING DEVICE FOR PROGRAM CONTROL UNIT AND METHOD THEREOF	
20	JP 4113166 81 A	☒	LOADING METHOD TO INSTRUCTION BUFFER AND DEVICE AND PROCESSOR THEREFOR	
21	JP 11289348 A	☒	PACKET EXCHANGE AND DATA TRANSMISSION PROCESSING METHOD THEREFOR	
22	JP 11259644 A	☒	IMAGE FORMING DEVICE AND IMAGE FORMING METHOD	
23	JP 11242599 A	☒	COMPUTER PROGRAM	
24	JP 11085619 A	☒	INFORMATION PROCESSOR	
25	JP 11073318 A	☒	MICROPROCESSOR	
26	JP 10307723 A	☒	PROCESSOR	
27	JP 10207708 A	☒	PROGRAMMABLE CONTROLLER	
28	JP 10177559 A	☒	DEVICE, METHOD, AND SYSTEM FOR PROCESSING DATA	
29	JP 10091436 A	☒	PROGRAM LOADER	
30	JP 10003425 A	☒	INSTRUCTION SUPPLY DEVICE	
31	JP 09274565 A	☒	PIPELINED MICROPROCESSOR WITH NO INTERRUPTION CAUSED BY BRANCH AND OPERATING METHOD FOR THE SAME	
32	JP 09251286 A	☒	DISPLAY GRAPHIC ADAPTER IN WINDOW SYSTEM FOR PROCESSING DIFFERENT PIXEL SIZES AND METHOD FOR STORING PIXEL DATA	
33	JP 09114660 A	☒	DATA PROCESSOR	
34	JP 09022354 A	☒	METHOD AND DEVICE FOR EXECUTING INSTRUCTION SEQUENCE	
35	JP 09006759 A	☒	VECTOR PROCESSOR	
36	JP 08314720 A	☒	BRANCH CONTROL SYSTEM	
37	JP 08249228 A	☒	DATA PROCESSOR	
38	JP 08110901 A	☒	MICROPROCESSOR	
39	JP 08095786 A	☒	ARITHMETIC PROCESSOR	

	Document ID	U	Title	Current OR
40	JP 07210 323 A	☒	DATA BATCH TRANSFER METHOD IN SEQUENTIAL ACCESS METHOD AND SECTION SEQUENTIAL ACCESS METHOD	
41	JP 07056 734 A	☒	MICROPROCESSOR AND CONTROL METHOD THEREOF	
42	JP 06309 167 A	☒	PROCESSOR FOR PARALLEL PROCESSING OF PLURAL INSTRUCTIONS	
43	JP 06242 954 A	☒	METHOD FOR IMPROVING INSTRUCTION DISPATCH IN SUPERSCALAR PROCESSOR SYSTEM BY USING INDEPENDENTLY ACCESSED INTERMEDIATE STORAGE AREA AND SYSTEM FOR THE SAME	
44	JP 06236 275 A	☒	METHOD AND SYSTEM FOR DISPATCHING AND EXECUTING NON-SEQUENTIAL INSTRUCTION IN A SUPERSCALAR PROCESSOR SYSTEM	
45	JP 06236 273 A	☒	METHOD AND SYSTEM FOR DISPATCHING A PLURALITY OF INSTRUCTIONS BY ONE CYCLE IN SUPERSCALAR PROCESSOR SYSTEM	
46	JP 06236 267 A	☒	METHOD AND SYSTEM FOR IMPROVING INSTRUCTION DISPATCHING EFFICIENCY IN SUPERSCALAR PROCESSOR	
47	JP 05324 477 A	☒	ADDRESS TRANSFORMATION BUFFER MECHANISM	
48	JP 05313 894 A	☒	INFORMATION PROCESSOR	
49	JP 05233 229 A	☒	INFORMATION PROCESSOR AND INFORMATION PROCESSING METHOD	
50	JP 05224 921 A	☒	DATA PROCESSING SYSTEM	
51	JP 05173 785 A	☒	INSTRUCTION PREFETCHING DEVICE	
52	JP 05100 883 A	☒	SEMICONDUCTOR DEVICE FOR PROCESSING DATA	
53	JP 05053 805 A	☒	ELECTRONIC COMPUTER	
54	JP 04361 329 A	☒	INSTRUCTION FETCH CIRCUIT	
55	JP 04326 127 A	☒	PARALLEL INSTRUCTION EXECUTION SYSTEM	
56	JP 04175 930 A	☒	DATA PROCESSOR	
57	JP 04153 733 A	☒	INSTRUCTION SUPPLY DEVICE OF PARALLEL PROCESSOR	
58	JP 04116 727 A	☒	INTERPRETER DEVICE	
59	JP 02289 097 A	☒	METHOD AND DEVICE FOR PICTURE DISPLAY DATA PROCESSING	
60	JP 02280 247 A	☒	INFORMATION PROCESSOR	
61	JP 02257 342 A	☒	INFORMATION PROCESSOR	
62	JP 02236 657 A	☒	INFORMATION PROCESSING SYSTEM	

	Document ID	U	Title	Current OR
63	JP 02118 833 A	☒	INSTRUCTION DECODER	
64	JP 02112 054 A	☒	DATA PROCESSOR	
65	JP 01292 437 A	☒	DATA DRIVING TYPE CONTROL METHOD	
66	JP 01283 640 A	☒	DATA DRIVING TYPE CONTROL METHOD	
67	JP 01126 733 A	☒	INFORMATION PROCESSOR	
68	JP 01123 549 A	☒	PACKET SWITCH	
69	JP 01044 545 A	☒	CENTRAL PROCESSING UNIT	
70	JP 63254 531 A	☒	INSTRUCTION READ CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
71	JP 63231 531 A	☒	PIPELINE CONTROLLER	
72	JP 63201 832 A	☒	PIPELINE PROCESSING TYPE INFORMATION PROCESSOR	
73	JP 63012 029 A	☒	INFORMATION PROCESSOR	
74	JP 62196 730 A	☒	STAGE CONTROL SYSTEM FOR DATA PROCESSOR	
75	JP 62133 532 A	☒	MICROPROCESSOR	
76	JP 62121 567 A	☒	DATA PROCESSOR	
77	JP 61122 754 A	☒	MICROPROCESSOR	
78	JP 60263 238 A	☒	INFORMATION PROCESSOR	
79	JP 60250 438 A	☒	INFORMATION PROCESSOR	
80	JP 60173 634 A	☒	INSTRUCTION SIGNAL TRAIN PROCESSING CIRCUIT	
81	JP 60124 738 A	☒	INITIAL SETTING AND DIAGNOSTIC CONTROLLING SYSTEM OF INFORMATION PROCESSING UNIT	
82	JP 58024 946 A	☒	OPERATING PROCESSING SYSTEM	
83	JP 57103 553 A	☒	INSTRUCTION READING SYSTEM	
84	JP 57029 154 A	☐	INSTRUCTION BUFFER CONTROLLING SYSTEM	
85	JP 56162 151 A	☐	INFORMATION PROCESSING DEVICE	

	Document ID	U	Title	Current OR
86	JP 54107 239 A	☐	PROGRAM EXECUTION ORDER CONTROL SYSTEM	
87	EP 12514 25 A2	☐	Very long instruction word information processing device and system	
88	EP 11071 11 A2	☐	System and method for register renaming	
89	EP 11071 09 A2	☐	Data processing device	
90	EP 10244 26 A2	☐	High performance RISC microprocessor architecture	
91	EP 99289 4 A1	☐	Apparatus and method for loop execution	
92	EP 99289 3 A1	☐	Verifying instruction parallelism	
93	EP 88620 9 A2	☐	Extensible risc microprocessor architecture	
94	EP 84966 5 A2	☐	System and method for register renaming	
95	EP 74024 8 A1	☐	Method and apparatus for detecting and executing traps in a superscalar processor	
96	EP 73791 5 A1	☐	Method and apparatus for improving system performance in a data processing system	
97	EP 64448 2 A1	☐	Dispatch of instructions to multiple execution units.	
98	WO 94163 84 A1	☐	SYSTEM AND METHOD FOR REGISTER RENAMING	
99	EP 60664 3 A1	☐	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system.	
100	EP 60587 5 A1	☐	Method and system for single cycle dispatch of multiple instruction in a superscalar processor system.	
101	EP 60586 8 A1	☐	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system.	
102	EP 60586 6 A1	☐	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage.	
103	WO 93227 22 A1	☐	A SYSTEM AND METHOD FOR RETIRING INSTRUCTIONS IN A SUPERSCALAR MICROPROCESSOR	
104	WO 93015 46 A1	☐	EXTENSIBLE RISC MICROPROCESSOR ARCHITECTURE	
105	WO 93015 45 A1	☐	HIGH-PERFORMANCE RISC MICROPROCESSOR ARCHITECTURE	
106	EP 47188 8 A2	☐	Microprocessor for enhancing initiation of data processing after execution of conditional branch instruction.	
107	EP 44849 9 A2	☐	Instruction prefetch method for branch-with-execute instructions.	
108	EP 30795 7 A2	☐	Central processing unit having instruction prefetch function.	

	Document ID	U	Title	Current OR
109	GB 2016753 A	☐	Data Processing System	
110	US 20030131162 A	☐	Non-destructive read FIFO memory device for multiple execution of instruction loops, has read pointer which is reset to address containing an instruction and then incremented to address of last instruction of loop	
111	JP 2003186684 A	☐	Dynamic waiting condition designation method of service logic program instance in intelligent network, involves designating maximum number of simultaneous execution of processes and length of waiting queue	
112	US 20030065905 A	☐	Parallel computation processor for high-speed loop operations has multiplexers which select either instructions dispatched from instruction dispatcher or instructions dispatched by instruction buffer operated by loop control unit	
113	US 6463524 B	☐	Multiple store instructions issuing method in superscalar data processing system, involves issuing selected address and data operands in single queue instruction slot to load/store and fixed point units, for execution	
114	WO 2002468887 A	☐	Concurrent multitasking processor for real-time operating system device, provides priority tags to instructions corresponding to selected tasks, in instruction queues and sends them to execution units	
115	US 6381689 B	☐	Superscalar microprocessor for computer system, has recorder buffer which allocates storage for instruction results corresponding to multiple concurrently dispatched instructions	
116	US 6324640 B	☐	Superscalar processor for use in data processing system, has delay register coupled to dispatch queue which dispatches several instruction groups and rename tables	
117	KR 2001002485 A	☐	Multi-thread microprocessor for instruction fetch	
118	EP 1050805 A	☐	Computer system for executing instructions with guard indicators, has supply circuit with main instruction queue to be supplied to parallel execution units and subsidiary instruction queue having priority access to execution pipelines	
119	US 6115807 A	☐	Static instruction decoder for superscalar processors, has timer indexed by pointer for indicating initial instruction to be issued in next clock cycle	
120	EP 992893 A	☐	Processor for executing instructions in parallel has instruction buffer and decoders storing and decoding two instructions and arbitration and merge logic arbitrating between instructions	
121	WO 9957638 A	☐	Parallel data access method - involves buffering data submitted by sequence controller and instruction decoder during clock cycle, in respective register of processor, forwarding data to execution unit and combining them with corresponding commands	
122	US 5870575 A	☐	Guest branch instruction emulating method in data processing system e.g. desktop computer system	
123	US 5850542 A	☐	Cache system for fetching instructions in data processor - includes branch resolution unit that fetches non-guessed instruction stream corresponding to branch instruction and identification tag, during specified clock cycle	
124	GB 2324392 A	☐	Thread switch latency decreasing method for multithread processor - involves storing active threads in primary instruction queue for concurrent execution, and dormant threads in thread switch instruction queue for non-concurrent execution	
125	JP 10207708 A	☐	Programmable controller for control of industrial apparatus, machine, FA apparatus - executes succession instruction parallelly during multiple cycle instruction execution based on added two tags and buffer pointer	

	Document ID	U	Title	Current OR
126	US 5787303 A	☐	Parallel processing system with arithmetic operation unit for executing very large instruction words - stops output of next VLIW from instruction buffer upon detection of no-operation state thereby delaying execution of next VLIW for instruction cycle	
127	JP 10105399 A	☐	Data processor with pipeline processing function - has instruction decoder that converts and outputs control signals of each function of pipeline, based on several simultaneously executable instructions detected from instruction buffer	
128	GB 2317724 A	☐	Multiple instruction parallel issue/execution management system - includes forward map buffer indicating whether instruction execution value result is to be used as input operand in other instruction	
129	JP 10003425 A	☐	Instruction input device for very long instruction word parallel computer - produces instruction code repeatedly with execution number, which is executed by parallel computer	
130	US 5617549 A	☐	Multiple instruction selection and buffering unit for CPU execution - has decoder generating bundle instruction indicating whether even and odd instruction pair can be executed simultaneously with selector routing instructions to operational units	
131	EP 829045 B	☐	Method of rotating queued and fetched instructions for parallel processing in microprocessor - involves rotating all fetched and non-issued instructions together into issue order before next issue cycle.	
132	US 5542058 A	☐	Single chip CPU for pipelined processor - includes instruction queue to sequentially buffer operands during instruction decoding, then removing operands during instruction execution	
133	EP 697650 A	☐	Instruction queue scanning for super-scalar CISC computer - using instruction cache feeding byte queue that is scanned to generate components relevant to each dispatch stage of RISC core processor	
134	EP 651321 A	☐	Super-scalar microprocessor - decodes integer and floating point instructions in same microprocessor cycle and has common register file for accepting instruction results	
135	US 5481743 A	☐	Minimal instruction set computer system with multiple instruction issuing - has memory with bidirectional data port and instruction buffer for storing multiple instructions to be executed in parallel by multiple processing units	
136	EP 646861 B	☐	History buffer system for allowing recovery of executed instructions - includes main history buffer with storage entries each having field for address of issued instruction, and tag field corresp. to subsidiary history buffer for storing control data	
137	EP 644482 A	☐	Computer system for dispatching instructions to multiple execution units - defines instructions as dependent or independent for execution sequentially or in parallel depending upon definition and relationship to other instructions	
138	EP 639810 A	☐	Temporary register storage for scalar processor - has multiple processors executing instructions and using rename buffers until control unit directs write back to general registers	
139	US 5335330 A	☐	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
140	EP 682789 B	☐	Register re-naming system for super-scalar reduced instruction set computers - assigns tag to each instruction in variable advance instruction window and stores results of instructions executed in buffer according to corresp tags	
141	EP 605868 A	☐	Instruction dispatching method for super-scalar processor system - involves using storage buffers for instructions which are dispatched between time that storage buffer has been assigned for specific general register and results of execution are moved	

	Document ID	U	Title	Current OR
142	EP 663083 B	☐	Load and store operation handling for superscalar processors - has load and store unit handling out of order requests, address collision detection and data alignment of eight unaligned data bytes	
143	EP 638183 B	☐	Retiring instructions in superscaler microprocessor - stores results of incomplete instructions in temporary registers and retires instructions when their results can be moved to register array	
144	EP 551173 A	☐	Dataflow architecture for computer - executes instructions according to instruction queue on outside and active operands and stores results as next active operand	
145	US 5212779 A	☐	Pipelined data processor for executing processing instruction in parallel - has number of microprograms stored in microprogram memory, microprogram counter, instruction decoding and executing stages and store buffer and selector	
146	US 5201057 A	☐	Central processing unit for computer - has instruction queue for storing series of instructions and processing elements for executing instructions and sink matrix storing results of execution of multiple interactions of instructions	
147	US 5185868 A	☐	Computer instruction executing appts. with pipelined architecture - sends instructions to executing unit according to logical sequence and shifts other instructions into vacant decoders	
148	EP 520572 A	☐	Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors	
149	EP 518420 A	☐	Computer system with multiple duplicate functional units for concurrent processing - has instruction issue unit with register files coupled by interconnection network to main memory and cache memory, to process out-of-order instructions	
150	DE 4211222 A	☐	Branch instruction target controller for super-scaling processor system - has branch target buffer providing tabulated group of instructions with instruction checking unit	
151	GB 2250840 A	☐	Extended branch target logic for microprocessor - executes branch instruction and is target instruction stored in branch target buffer to be executed concurrently, minimising delay in pipeline processor	
152	EP 453268 A	☐	Microprocessor for inserting bus cycle to output internal information - has bus controller coupled to other processors to enable insertion of bus cycle in accordance with bus cycle request signal	
153	US 5226130 A	☐	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
154	EP 438038 B	☐	Graphic processor for picture screen - converts general graphic instructions to sequence of primitive pixel orientated instructions for storage in queue memory	
155	EP 413434 A	☐	Pipelined processor with variable instruction length - has latch circuit holding instruction preceding each instruction memory access to quickly provide variable length instructions	
156	EP 381471 A	☐	Multiple instruction pre-processor - resolves data dependencies during pre-processing of multiple instructions prior to execution of those instructions in digital computer	
157	EP 380859 A	☐	Source list, pointer queues and result queues - resolving data dependency during pre-processing of multiple instructions prior to execution of those instructions in digital computer	
158	EP 360553 A	☐	Write-back system maintaining identity between buffer and main store - has duplicated buffer store and move-out buffers arranged to transfer two halves of data concurrently	
159	AU 8823438 A	☐	Prefetching queue control system - has instruction read out from memory and stored in buffer with write and transfer devices for prefetching parallel to instruction execution	
160	US 4816991 A	☐	VM system for holding host and multiple guest entries - has address translation look-aside buffer, and instruction execution unit to command start by setting CPU to necessary fields of guest	

	Document ID	U	Title	Current OR
161	EP 268264 A	☐	High speed pipelined - indicates when control instruction is decoded and serialisation element is to be input to necessary units	
162	US 4736292 A	☐	Electronic data processing method overlaid jump insertion - having jump target instruction and corresp. control word portion concurrently written over instruction	
163	EP 239097 A	☐	Data processing system with decoded instruction queue memory - has queue structure composed of entries for latching entry information and including up=down counter	
164	EP 239081 A	☐	Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed	
165	DE 3586235 G	☐	Instruction prefetch operation for branch instructions - by generating control tag whose current value is changed each time branch instruction is reached	
166	US 4561052 A	☐	Instruction pre-fetch system for pipelining information processor - has control logic that moves instruction addresses through selector, instruction buffer and logical and physical address generator	
167	EP 118828 A	☐	Instruction fetch look-aside buffer for data processing - reduces fetches from storage under loop mode control by extracting instructions directly from the buffer	
168	EP 108338 A	☐	Parallel queuing method for multiprocessor data processing system - providing lock for de-queuing any element and which is examined by that program routine to delete but not insert anchor-pointed element	
169	EP 106670 A	☐	Digital data processor with multiple execution units - has operation code identifying each instruction issued in program order to queue of collector, and results stored in stack	
170	DE 3247196 A	☐	Microprocessor operating system - provides simultaneous execution of multiple programs so that programs are polled successively and instructions and data are queued	
171	EP 360935 A	☐	Information processing system with single chip arithmetic control unit - preventing malfunction by rendering content of instruction buffers ineffective and rewritten under certain conditions	

	Document ID	U	Title	Current OR
1	US 20040054872 A1	☐	High-performance, superscalar-based computer system with out-of-order intstruction execution	712/206
2	US 20040044878 A1	☒	Synchronisation between pipelines in a data processing apparatus	712/34
3	US 20040003216 A1	☒	Branch prediction apparatus and method	712/237
4	US 20030188139 A1	☒	Flexible demand-based resource allocation for multiple requestors in a simultaneous multi-threaded CPU	712/225
5	US 20030163671 A1	☒	Method and apparatus for prioritized instruction issue queue	712/214
6	US 20030120900 A1	☒	Apparatus and method for a software pipeline loop procedure in a digital signal processor	712/215
7	US 20030110201 A1	☒	VLIW instruction control	718/102
8	US 20030079113 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
9	US 20030074546 A1	☒	Data processing apparatus	712/241
10	US 20030070060 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
11	US 20030065905 A1	☒	Parallel computation processor, parallel computation control method and program thereof	712/23
12	US 20030056087 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
13	US 20030056086 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
14	US 20030043156 A1	☒	Apparatus and method for extracting and loading data to/from a buffer	345/537
15	US 20030040814 A1	☒	Method for controlling mechanisms and technical systems a corresponding device and control software	700/42
16	US 20030039248 A1	☒	System and method for the consolidation of data packets	370/392
17	US 20020174385 A1	☒	Computer system with debug facility	714/38

	Document ID	U	Title	Current OR
18	US 20020 15699 2 A1	☒	Information processing device and computer system	712/24
19	US 20020 02932 8 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
20	US 20010 04977 0 A1	☒	BUFFER MEMORY MANAGEMENT IN A SYSTEM HAVING MULTIPLE EXECUTION ENTITIES	711/129
21	US 20010 04219 2 A1	☒	Mechanism for self-initiated instruction issuing and method therefor	712/215
22	US 20010 02523 7 A1	☒	Computer system with debug facility	703/26
23	US 66717 94 B1	☒	Address generation interlock detection	712/217
24	US 66657 96 B1	☒	Microprocessor instruction result obfuscation	713/190
25	US 66314 59 B1	☒	Extended instruction word folding apparatus	712/210
26	US 66092 47 B1	☒	Method and apparatus for re-creating the trace of an emulated instruction set when executed on hardware native to a different instruction set field	717/128
27	US 65981 52 B1	☒	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
28	US 65052 95 B1	☒	Data processor	712/241
29	US 63306 57 B1	☒	Pairing of micro instructions in the instruction queue	712/23
30	US 63082 60 B1	☒	Mechanism for self-initiated instruction issuing and method therefor	712/215
31	US 63026 98 B1	☒	Method and apparatus for on-line teaching and learning	434/323
32	US 62956 00 B1	☒	Thread switch on blocked load or store using instruction thread field	712/228
33	US 62470 64 B1	☒	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312
34	US 62090 81 B1	☒	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system	712/215
35	US 61087 66 A	☒	Structure of processor having a plurality of main processors and sub processors, and a method for sharing the sub processors	712/34
36	US 60818 87 A	☒	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
37	US 60386 53 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
38	US 59564 95 A	☒	Method and system for processing branch instructions during emulation in a data processing system	703/26

	Document ID	U	Title	Current OR
39	US 5941984 A	☒	Data processing device	712/218
40	US 5920710 A	☒	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
41	US 5903741 A	☒	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
42	US 5898882 A	☒	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage	712/23
43	US 5894582 A	☒	Method of controlling parallel processing at an instruction level and processor for realizing the method	712/23
44	US 5894575 A	☒	Method and system for initial state determination for instruction trace reconstruction	717/128
45	US 5870579 A	☒	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
46	US 5870575 A	☒	Indirect unconditional branches in data processing system emulation mode	712/209
47	US 5784604 A	☒	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
48	US 5675676 A	☒	Data processor using FIFO memories for routing operations to parallel operational units	712/220
49	US 5574939 A	☒	Multiprocessor coupling system with integrated compile and run time scheduling for parallelism	712/24
50	US 5491829 A	☒	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system	712/23
51	US 5465373 A	☒	Method and system for single cycle dispatch of multiple instructions in a superscalar processor system	712/215
52	US 5465372 A	☒	Dataflow computer for following data dependent path processes	712/25
53	US 5452427 A	☒	Data processing device for variable word length instruction system having short instruction execution time and small occupancy area	712/210
54	US 5437017 A	☒	Method and system for maintaining translation lookaside buffer coherency in a multiprocessor data processing system	709/213
55	US 5404471 A	☒	Method and apparatus for switching address generation modes in CPU having plural address generation modes	712/207
56	US 5381532 A	☒	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
57	US 5349656 A	☒	Task scheduling method in a multiprocessor system where task selection is determined by processor identification and evaluation information	718/102
58	US 5335330 A	☒	Information processing apparatus with optimization programming	712/241
59	US 4893233 A	☒	Method and apparatus for dynamically controlling each stage of a multi-stage pipelined data unit	712/244
60	US 4766566 A	☒	Performance enhancement scheme for a RISC type VLSI processor using dual execution units for parallel instruction processing	712/23
61	US 4561052 A	☒	Instruction prefetch system	712/207

	Document ID	U	Title	Current OR
62	US 4532589 A	☒	Digital data processor with two operation units	712/217
63	US 4231106 A	☒	Performance monitor apparatus and method	702/186
64	US 4200927 A	☒	Multi-instruction stream branch processing mechanism	712/235
65	US 4172284 A	☐	Priority interrupt apparatus employing a plural stage shift register having separate interrupt mechanisms coupled to the different stages thereof for segregating interrupt requests according to priority levels	710/264

	Document ID	U	Title	Current OR
1	JP 20023 18687 A	☐	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
2	JP 20020 41284 A	☒	DEVICE FOR CONTRACTING EXTENDED INSTRUCTION WORD	
3	JP 20023 18687 A	☒	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
4	JP 20020 41284 A	☒	DEVICE FOR CONTRACTING EXTENDED INSTRUCTION WORD	
5	JP 20001 81709 A	☒	INSTRUCTION CONTROLLER	
6	JP 10091 436 A	☒	PROGRAM LOADER	
7	JP 09198 374 A	☒	VECTOR PROCESSOR	
8	JP 08055 026 A	☒	DATA PROCESSOR	
9	JP 06332 701 A	☒	INFORMATION PROCESSOR	
10	JP 06236 275 A	☒	METHOD AND SYSTEM FOR DISPATCHING AND EXECUTING NON-SEQUENTIAL INSTRUCTION IN A SUPERSCALAR PROCESSOR SYSTEM	
11	JP 06236 267 A	☒	METHOD AND SYSTEM FOR IMPROVING INSTRUCTION DISPATCHING EFFICIENCY IN SUPERSCALAR PROCESSOR	
12	JP 06161 745 A	☒	METHOD AND DEVICE FOR VERIFYING DATA PROCESSOR	
13	JP 03188 530 A	☒	PROGRAM PREFETCHING DEVICE	
14	JP 02118 833 A	☒	INSTRUCTION DECODER	
15	JP 62031 439 A	☒	INSTRUCTION REPROCESSING CONTROL SYSTEM	
16	JP 60263 238 A	☒	INFORMATION PROCESSOR	
17	JP 60124 738 A	☒	INITIAL SETTING AND DIAGNOSTIC CONTROLLING SYSTEM OF INFORMATION PROCESSING UNIT	
18	EP 12514 25 A2	☒	Very long instruction word information processing device and system	
19	EP 60587 5 A1	☒	Method and system for single cycle dispatch of multiple instruction in a superscalar processor system.	
20	EP 60586 8 A1	☒	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system.	
21	EP 60586 6 A1	☒	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage.	

	Document ID	U	Title	Current OR
22	EP 471888 A2	☒	Microprocessor for enhancing initiation of data processing after execution of conditional branch instruction.	
23	US 20030065905 A	☒	Parallel computation processor for high-speed loop operations has multiplexers which select either instructions dispatched from instruction dispatcher or instructions dispatched by instruction buffer operated by loop control unit	
24	EP 1251425 A	☒	Information processor e.g. computer system has controller which selects predetermined number of instructions from instruction buffer, and transmits to another buffer for executing instructions in parallel	
25	WO 2002466887 A	☒	Concurrent multitasking processor for real-time operating system device, provides priority tags to instructions corresponding to selected tasks, in instruction queues and sends them to execution units	
26	US 5870575 A	☒	Guest branch instruction emulating method in data processing system e.g. desktop computer system	
27	GB 2324392 A	☒	Thread switch latency decreasing method for multithread processor - involves storing active threads in primary instruction queue for concurrent execution, and dormant threads in thread switch instruction queue for non-concurrent execution	
28	US 5335330 A	☒	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
29	US 5263169 A	☒	Bus arbitration and re source management for signal processor - has processor arbiter which supervises on priority basis both captive processor resources and independent processor resources	
30	EP 551173 A	☒	Dataflow architecture for computer - executes instructions according to instruction queue on outside and active operands and stores results as next active operand	
31	EP 520572 A	☒	Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors	
32	GB 2250840 A	☒	Extended branch target logic for microprocessor - executes branch instruction and is target instruction stored in branch target buffer to be executed concurrently, minimising delay in pipeline processor	
33	EP 413434 A	☒	Pipelined processor with variable instruction length - has latch circuit holding instruction preceding each instruction memory access to quickly provide variable length instructions	
34	BR 8804969 A	☒	Multiple instruction stream multiple data pipelined processing appts. - includes pipelined processors connected to receiver for temporarily holding incoming instructions	
35	EP 239081 A	☒	Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed	
36	US 4561052 A	☒	Instruction pre-fetch system for pipelining information processor - has control logic that moves instruction addresses through selector, instruction buffer and logical and physical address generator	
37	DE 3247196 A	☐	Microprocessor operating system - provides simultaneous execution of multiple programs so that programs are polled successively and instructions and data are queued	

	Document ID	U	Title	Current OR
1	US 20040064653 A1	☐	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/145
2	US 20030182511 A1	☒	Apparatus and method for resolving an instruction conflict in a software pipeline nested loop procedure in a digital signal processor	711/125
3	US 20030159019 A1	☒	Prediction of instructions in a data processing apparatus	712/207
4	US 20030154469 A1	☒	Apparatus and method for improved execution of a software pipeline loop procedure in a digital signal processor	717/161
5	US 20030120905 A1	☒	Apparatus and method for executing a nested loop program with a software pipeline loop procedure in a digital signal processor	712/241
6	US 20030120899 A1	☒	Apparatus and method for processing an interrupt in a software pipeline loop procedure in a digital signal processor	712/214
7	US 20030120882 A1	☒	Apparatus and method for exiting from a software pipeline loop procedure in a digital signal processor	711/169
8	US 20030034544 A1	☒	Microcomputer	257/523
9	US 20030016224 A1	☒	Display apparatus in which recovery time is short in fault occurence	345/506
10	US 20020199083 A1	☒	High code-density microcontroller architecture with changeable instruction formats	712/209
11	US 20020184479 A1	☒	Bytecode instruction processor with switch instruction handling logic	712/236
12	US 20020129208 A1	☒	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
13	US 20020124144 A1	☒	Scalable multiprocessor system and cache coherence method implementing store-conditional memory transactions while an associated directory entry is encoded as a coarse bit vector	711/145
14	US 20020124143 A1	☒	System and method for generating cache coherence directory entries and error correction codes in a multiprocessor system	711/145
15	US 20020112122 A1	☒	Verifying cumulative ordering	711/119
16	US 20020087807 A1	☒	System for minimizing directory information in scalable multiprocessor systems with logically independent input/output nodes	711/141
17	US 20020087806 A1	☒	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141

	Document ID	U	Title	Current OR
18	US 20020 08327 4 A1	☒	Scalable multiprocessor system and cache coherence method incorporating invalid-to-dirty requests	711/144
19	US 20020 04632 7 A1	☒	Cache coherence protocol engine and method for processing memory transaction in distinct address subsets during interleaved time periods in a multiprocessor system	711/141
20	US 20020 02044 4 A1	☒	Automatically switching valve with remote signaling	137/112
21	US 20020 01690 3 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
22	US 20020 01084 0 A1	☒	Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants	711/141
23	US 20020 00744 3 A1	☒	Scalable multiprocessor system and cache coherence method	711/141
24	US 20020 00743 9 A1	☒	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/119
25	US 20010 03230 7 A1	☒	MICRO-INSTRUCTION QUEUE FOR A MICROPROCESSOR INSTRUCTION PIPELINE	712/219
26	US 20010 02751 3 A1	☒	Parallel processor and image processing system using the processor	712/22
27	US 67082 96 B1	☒	Method and system for selecting and distinguishing an event sequence using an effective address in a processing system	714/47
28	US 67014 84 B1	☒	Register file with delayed parity check	714/801
29	US 66979 19 B2	☒	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/141
30	US 66752 65 B2	☒	Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants	711/141
31	US 66402 87 B2	☒	Scalable multiprocessor system and cache coherence method incorporating invalid-to-dirty requests	711/141
32	US 66369 49 B2	☒	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
33	US 66257 56 B1	☒	Replay mechanism for soft error recovery	714/17
34	US 66222 36 B1	☒	Microprocessor instruction fetch unit for processing instruction groups having multiple branch instructions	712/206
35	US 66222 18 B2	☒	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
36	US 66222 17 B2	☒	Cache coherence protocol engine system and method for processing memory transaction in distinct address subsets during interleaved time periods in a multiprocessor system	711/141
37	US 66112 69 B1	☒	Video display unit and program recording medium	345/522

	Document ID	U	Title	Current OR
38	US 6578134 B1	☒	Multi-branch resolution	712/219
39	US 6560695 B1	☒	Dynamic pipe staging adder	712/214
40	US 6536456 B2	☒	Automatically switching valve with remote signaling	137/12
41	US 6529509 B1	☒	Switch controlling apparatus for small capacitance ATM exchange	370/395.4
42	US 6499116 B1	☒	Performance of data stream touch events	714/39
43	US 6484256 B1	☒	Apparatus and method of branch prediction utilizing a comparison of a branch history table to an aliasing table	712/240
44	US 6477654 B1	☒	Managing VT for reduced power using power setting commands in the instruction stream	713/300
45	US 6449710 B1	☒	Stitching parcels	712/216
46	US 6414368 B1	☒	Microcomputer with high density RAM on single chip	257/523
47	US 6412064 B1	☒	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
48	US 6351796 B1	☒	Methods and apparatus for increasing the efficiency of a higher level cache by selectively performing writes to the higher level cache	711/204
49	US 6334184 B1	☒	Processor and method of fetching an instruction that select one of a plurality of decoded fetch addresses generated in parallel to form a memory request	712/235
50	US 6311267 B1	☒	Just-in-time register renaming technique	712/217
51	US 6282630 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
52	US 6275903 B1	☒	Stack cache miss handling	711/132
53	US 6266767 B1	☒	Apparatus and method for facilitating out-of-order execution of load instructions	712/217
54	US 6266761 B1	☒	Method and system in an information processing system for efficient maintenance of copies of values stored within registers	712/23
55	US 6249855 B1	☒	Arbiter system for central processing unit having dual dominoed encoders for four instruction issue per machine cycle	712/23
56	US 6240510 B1	☒	System for processing a cluster of instructions where the instructions are issued to the execution units having a priority order according to a template associated with the cluster of instructions	712/236
57	US 6237086 B1	☒	1 Method to prevent pipeline stalls in superscalar stack based computing systems	712/226
58	US 6237077 B1	☒	Instruction template for efficient processing clustered branch instructions	712/24
59	US 6216206 B1	☒	Trace victim cache	711/133

	Document ID	U	Title	Current OR
60	US 6212619 B1	☒	System and method for high-speed register renaming by counting	712/23
61	US 6209073 B1	☒	System and method for interlocking barrier operations in load and store queues	711/169
62	US 6189072 B1	☒	Performance monitoring of cache misses and instructions completed for instruction parallelism analysis	711/118
63	US 6170050 B1	☒	Length decoder for variable length data	712/210
64	US 6170038 B1	☒	Trace based instruction caching	711/125
65	US 6131157 A	☒	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
66	US 6128720 A	☒	Distributed processing array with component processors performing customized interpretation of instructions	712/20
67	US 6108768 A	☒	Reissue logic for individually reissuing instructions trapped in a multiissue stack based computing system	712/214
68	US 6105128 A	☒	Method and apparatus for dispatching instructions to execution units in waves	712/215
69	US 6085338 A	☒	CPI infinite and finite analysis	714/47
70	US 6079002 A	☒	Dynamic expansion of execution pipeline stages	711/169
71	US 6076144 A	☒	Method and apparatus for identifying potential entry points into trace segments	711/125
72	US 6073213 A	☒	Method and apparatus for caching trace segments with multiple entry points	711/125
73	US 6061767 A	☒	Processor with pipelining structure and method for high-speed calculation with pipelining processors	370/535
74	US 6049882 A	☒	Apparatus and method for reducing power consumption in a self-timed system	713/322
75	US 6041167 A	☒	Method and system for reordering instructions after dispatch in a processing system	712/214
76	US 6029006 A	☒	Data processor with circuit for regulating instruction throughput while powered and method of operation	713/323
77	US 6023756 A	☒	Instruction processing method and system for variable-length instructions	712/208
78	US 6021261 A	☒	Method and system for testing a multiprocessor data processing system utilizing a plurality of event tracers	714/37
79	US 6018786 A	☒	Trace based instruction caching	711/4
80	US 6006309 A	☒	Information block transfer management in a multiprocessor computer system employing private caches for individual center processor units and a shared cache	711/123
81	US 5987616 A	☒	Semiconductor device	713/320
82	US 5978896 A	☒	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23

	Document ID	U	Title	Current OR
83	US 5974535 A	☒	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
84	US 5970439 A	☒	Performance monitoring in a data processing system	702/186
85	US 5963973 A	☒	Multiprocessor computer system incorporating method and apparatus for dynamically assigning ownership of changeable data	711/130
86	US 5961654 A	☒	Operand fetch bandwidth analysis	714/47
87	US 5958041 A	☒	Latency prediction in a pipelined microarchitecture	712/214
88	US 5951679 A	☒	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
89	US 5949971 A	☒	Method and system for performance monitoring through identification of frequency and length of time of execution of serialization instructions in a processing system	714/47
90	US 5941962 A	☒	Buffer management system for releasing a buffer area based on holding time and maximum allowable time when remaining buffer areas reached threshold	710/53
91	US 5938760 A	☒	System and method for performance monitoring of instructions in a re-order buffer	712/220
92	US 5930508 A	☒	Method for storing and decoding instructions for a microprocessor having a plurality of function units	717/158
93	US 5930495 A	☒	Method and system for processing a first instruction in a first processing environment in response to intiating processing of a second instruction in a emulation environment	703/26
94	US 5928355 A	☒	Apparatus for reducing instruction issue stage stalls through use of a staging register	712/214
95	US 5925122 A	☒	Data processing unit which pre-fetches instructions of different lengths to conduct processing	712/210
96	US 5922069 A	☒	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
97	US 5922068 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215
98	US 5918034 A	☒	Method for decoupling pipeline stages	712/218
99	US 5913054 A	☒	Method and system for processing a multiple-register instruction that permit multiple data words to be written in a single processor cycle	712/220
100	US 5906002 A	☒	Method and apparatus for saving and restoring the context of registers using different instruction sets for different sized registers	711/171
101	US 5900025 A	☒	Processor having a hierarchical control register file and methods for operating the same	712/248
102	US 5900012 A	☒	Storage device having varying access times and a superscalar microprocessor employing the same	711/120
103	US 5898852 A	☒	Load instruction steering in a dual data cache microarchitecture	712/214
104	US 5897655 A	☒	System and method for cache replacement within a cache set based on valid, modified or least recently used status in order of preference	711/134
105	US 5895486 A	☒	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121

	Document ID	U	Title	Current OR
106	US 5881306 A	☒	Instruction fetch bandwidth analysis	712/23
107	US 5878208 A	☒	Method and system for instruction trace reconstruction utilizing limited output pins and bus monitoring	714/38
108	US 5870616 A	☒	System and method for reducing power consumption in an electronic circuit	713/324
109	US 5870612 A	☒	Method and apparatus for condensed history buffer	710/260
110	US 5870582 A	☒	Method and apparatus for completion of non-interruptible instructions before the instruction is dispatched	712/218
111	US 5870580 A	☒	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
112	US 5862371 A	☒	Method and system for instruction trace reconstruction utilizing performance monitor outputs and bus monitoring	712/228
113	US 5860026 A	☒	Information processing system for controlling operations of input/output devices of another clusters according to control instructions issued from a cluster	710/33
114	US 5860014 A	☒	Method and apparatus for improved recovery of processor state using history buffer	710/260
115	US 5845106 A	☒	Method for simulating cache operation	703/21
116	US 5835702 A	☒	Performance monitor	714/39
117	US 5832292 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
118	US 5829879 A	☒	Temperature sensor	374/178
119	US 5829029 A	☒	Private cache miss and access management in a multiprocessor system with shared memory	711/133
120	US 5828860 A	☒	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
121	US 5826055 A	☒	System and method for retiring instructions in a superscalar microprocessor	712/218
122	US 5809320 A	☒	High-performance multi-processor having floating point unit	712/34
123	US 5809268 A	☒	Method and system for tracking resource allocation within a processor	712/200
124	US 5805916 A	☒	Method and apparatus for dynamic allocation of registers for intermediate floating-point results	712/23
125	US 5805907 A	☒	System and method for reducing power consumption in an electronic circuit	713/300
126	US 5805906 A	☒	Method and apparatus for writing information to registers in a data processing system using a number of registers for processing instructions	710/260
127	US 5805777 A	☒	Data processor with branch target address cache and method of operation	712/239
128	US 5805475 A	☒	Load-store unit and method of loading and storing single-precision floating-point registers in a double-precision architecture	708/204

	Document ID	U	Title	Current OR
129	US 5802556 A	☒	Method and apparatus for correcting misaligned instruction data	711/109
130	US 5802273 A	☒	Trailing edge analysis	714/47
131	US 5797019 A	☒	Method and system for performance monitoring time lengths of disabled interrupts in a processing system	710/262
132	US 5784632 A	☒	Parallel diagonal-fold array processor	712/11
133	US 5784606 A	☒	Method and system in a superscalar data processing system for the efficient handling of exceptions	712/244
134	US 5765208 A	☒	Method of speculatively executing store instructions prior to performing snoop operations	711/204
135	US 5765199 A	☒	Data processor with alocate bit and method of operation	711/168
136	US 5761723 A	☒	Data processor with branch prediction and method of operation	711/144
137	US 5754811 A	☒	Instruction dispatch queue for improved instruction cache to queue timing	712/214
138	US 5752062 A	☒	Method and system for performance monitoring through monitoring an order of processor events during execution in a processing system	714/37
139	US 5751945 A	☒	Method and system for performance monitoring stalls to identify pipeline bottlenecks and stalls in a processing system	714/47
140	US 5748855 A	☒	Method and system for performance monitoring of misaligned memory accesses in a processing system	712/23
141	US 5745726 A	☒	Method and apparatus for selecting the oldest queued instructions without data dependencies	712/216
142	US 5732005 A	☒	Single-precision, floating-point register array for floating-point units performing double-precision operations by emulation	708/495
143	US 5729726 A	☒	Method and system for performance monitoring efficiency of branch unit operation in a processing system	712/233
144	US 5715427 A	☒	Semi-associative cache with MRU/LRU replacement	711/136
145	US 5715420 A	☒	Method and system for efficient memory management in a data processing system utilizing a dual mode translation lookaside buffer	711/206
146	US 5699538 A	☒	Efficient firm consistency support mechanisms in an out-of-order execution superscaler multiprocessor	712/23
147	US 5691920 A	☒	Method and system for performance monitoring of dispatch unit efficiency in a processing system	702/186
148	US 5687349 A	☒	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
149	US 5682544 A	☒	Massively parallel diagonal-fold tree array processor	712/16
150	US 5682495 A	☒	Fully associative address translation buffer having separate segment and page invalidation	711/207
151	US 5671382 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215

	Document ID	U	Title	Current OR
152	US 5668984 A	☒	Variable stage load path and method of operation	712/222
153	US 5664215 A	☒	Data processor with an execution unit for performing load instructions and method of operation	712/23
154	US 5663959 A	☒	ATM cell switching apparatus having a control cell bypass route	370/236.2
155	US 5655096 A	☒	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
156	US 5644779 A	☒	Processing system and method of operation for concurrent processing of branch instructions with cancelling of processing of a branch instruction	712/23
157	US 5621896 A	☒	Data processor with unified store queue permitting hit under miss memory accesses	711/118
158	US 5613081 A	☒	Method of operating a data processor with rapid address comparison for data forwarding	711/3
159	US 5606682 A	☒	Data processor with branch target address cache and subroutine return address cache and method of operation	711/204
160	US 5604879 A	☒	Single array address translator with segment and page invalidate ability and method of operation	711/207
161	US 5579493 A	☒	System with loop buffer and repeat control circuit having stack for storing control information	712/207
162	US 5560032 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
163	US 5559976 A	☒	System for instruction completion independent of result write-back responsive to both exception free completion of execution and completion of all logically prior instructions	712/215
164	US 5553255 A	☒	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
165	US 5550995 A	☒	Memory cache with automatic alliased entry invalidation and method of operation	711/3
166	US 5550974 A	☒	Testable memory array which is immune to multiple wordline assertions during scan testing	714/42
167	US 5548738 A	☒	System and method for processing an instruction in a processing system	712/215
168	US 5546599 A	☒	Processing system and method of operation for processing dispatched instructions with detected exceptions	712/23
169	US 5537602 A	☒	Process system for controlling bus system to communicate data between resource and processor	712/38
170	US 5535410 A	☒	Parallel processor having decoder for selecting switch from the group of switches and concurrently inputting MIMD instructions while performing SIMD operation	712/20
171	US 5535351 A	☒	Address translator with by-pass circuit and method of operation	711/207
172	US 5535346 A	☒	Data processor with future file with parallel update and method of operation	712/217
173	US 5530825 A	☒	Data processor with branch target address cache and method of operation	711/213
174	US 5530824 A	☒	Address translation circuit	711/207

	Document ID	U	Title	Current OR
175	US 5530822 A	☒	Address translator and method of operation	711/207
176	US 5524224 A	☒	System for speculatively executing instructions wherein mispredicted instruction is executed prior to completion of branch processing	712/219
177	US 5511172 A	☒	Speculative execution processor	712/235
178	US 5506437 A	☒	Microcomputer with high density RAM in separate isolation well on single chip	257/373
179	US 5491359 A	☒	Microcomputer with high density ram in separate isolation well on single chip	257/373
180	US 5488730 A	☒	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
181	US 5481689 A	☐	Conversion of internal processor register commands to I/O space addresses	711/202
182	US 5471591 A	☒	Combined write-operand queue and read-after-write dependency scoreboard	712/217
183	US 5452467 A	☒	Microcomputer with high density ram in separate isolation well on single chip	716/1
184	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
185	US 5394529 A	☒	Branch prediction unit for high-performance processor	712/240
186	US 5392228 A	☒	Result normalizer and method of operation	708/205
187	US 5386519 A	☒	Information processing apparatus incorporating buffer storing a plurality of branch target instructions for branch instructions and interrupt requests	712/238
188	US 5363495 A	☒	Data processing system with multiple execution units capable of executing instructions out of sequence	713/500
189	US 5353426 A	☒	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
190	US 5333296 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171
191	US 5317720 A	☒	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
192	US 5251306 A	☒	Apparatus for controlling execution of a program in a computing device	712/217
193	US 5247624 A	☒	Microprogram controller including leading microinstruction from a generator executed while succeeding microinstruction from memory is read out	712/211
194	US 5243698 A	☒	Microcomputer	709/201
195	US 5201057 A	☒	System for extracting low level concurrency from serial instruction streams	712/18
196	US 5197137 A	☒	Computer architecture for the concurrent execution of sequential programs	718/107
197	US 5197136 A	☒	Processing system for branch instruction	712/238

	Document ID	U	Title	Current OR
198	US 5185873 A	☒	Control system with flag indicating two or less data inputs and counter indicating two or more controlling data driven execution method	712/201
199	US 5185868 A	☒	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
200	US 5155843 A	☒	Error transition mode for multi-processor system	714/5

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030070062 A1	☐	System and method for reducing computing system latencies associated with branch instructions	712/234
2	US 20030070060 A1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
3	US 20030065905 A1	☐	Parallel computation processor, parallel computation control method and program thereof	712/23
4	US 20030061470 A1	☐	Power consumption reduction mechanism for pipeline stalls	712/219
5	US 20030061467 A1	☐	Scoreboarding mechanism in a pipeline that includes replays and redirects	712/217
6	US 20030061465 A1	☐	Issue and retirement mechanism in processor having different pipeline lenghths	712/214
7	US 20030061224 A1	☐	Processing system	707/100
8	US 20030058876 A1	☐	Methods and apparatus for retaining packet order in systems utilizing multiple transmit queues	370/412
9	US 20030056089 A1	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/225
10	US 20030056087 A1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
11	US 20030056086 A1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
12	US 20030046563 A1	☐	Encryption-based security protection for processors	713/190
13	US 20030043855 A1	☐	COMMUNICATION NETWORK, AND NODE DEVICE USED THEREIN AND CONTROL METHOD THEREFOR	370/503
14	US 20030043156 A1	☐	Apparatus and method for extracting and loading data to/from a buffer	345/537
15	US 20030040814 A1	☐	Method for controlling mechanisms and technical systems a corresponding device and control software	700/42
16	US 20030039248 A1	☐	System and method for the consolidation of data packets	370/392
17	US 20030033511 A1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235

	Document ID	U	Title	Current OR
18	US 20030033510 A1	☐	Methods and apparatus for controlling speculative execution of instructions based on a multiaccess memory condition	712/235
19	US 20030033505 A1	☐	Apparatus for processing instructions in a computing system	712/215
20	US 20030033336 A1	☐	Methods for efficient filtering of data	708/300
21	US 20030023959 A1	☐	General and efficient method for transforming predicated execution to static speculation	717/151
22	US 20030023835 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on dispatch of a quantity of instruction information for a full instruction	712/214
23	US 20030023834 A1	☐	Method and system to insert a flow marker into an instruction stream to indicate a thread switching operation within a multithreaded processor	712/214
24	US 20030023659 A1	☐	Method and apparatus for thread switching within a multithreaded processor	718/102
25	US 20030023658 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of the absence of a flow of instruction information for a thread	718/102
26	US 20030018687 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a flow marker within an instruction information	718/102
27	US 20030018686 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a stall condition	718/102
28	US 20030018685 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a branch instruction	718/102
29	US 20030009727 A1	☐	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
30	US 20030009622 A1	☐	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/118
31	US 20030005263 A1	☐	Shared resource queue for simultaneous multithreaded processing	712/218
32	US 20020194457 A1	☐	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
33	US 20020194456 A1	☐	System and method for register renaming	712/217
34	US 20020188829 A1	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/218

	Document ID	U	Title	Current OR
35	US 20020 18447 9 A1	☐	Bytecode instruction processor with switch instruction handling logic	712/236
36	US 20020 18447 6 A1	☐	Instructions for ordering execution in pipelined processes	712/225
37	US 20020 17834 7 A1	☐	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
38	US 20020 17653 5 A1	☐	Method and system monitoring image detection	378/62
39	US 20020 17438 5 A1	☐	Computer system with debug facility	714/38
40	US 20020 16994 5 A1	☐	Microprocessor	712/205
41	US 20020 16198 7 A1	☐	System and method including distributed instruction buffers holding a second instruction form	712/205
42	US 20020 15699 2 A1	☐	Information processing device and computer system	712/24
43	US 20020 14404 1 A1	☐	Early exception detection	710/260
44	US 20020 13366 1 A1	☐	Data processing system and microcomputer	710/308
45	US 20020 12082 9 A1	☐	Data processer and data processing system	712/207
46	US 20020 12081 3 A1	☐	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/118
47	US 20020 10802 9 A1	☐	Program counter (PC) relative addressing mode with fast displacement	712/234
48	US 20020 09992 8 A1	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/216
49	US 20020 09992 4 A1	☐	Processor	712/24
50	US 20020 09992 2 A1	☐	DATA PROCESSING APPARATUS INCLUDING A PLURALITY OF PIPELINE PROCESSING MECHANISMS IN WHICH MEMORY ACCESS INSTRUCTIONS ARE CARRIED OUT IN A MEMORY ACCESS PIPELINE	712/3
51	US 20020 09991 0 A1	☐	High speed low power cacheless computer system	711/117

	Document ID	U	Title	Current OR
52	US 20020095668 A1	☐	Compiler and register allocation method	717/157
53	US 20020095666 A1	☐	Program optimization method, and compiler using the same	717/149
54	US 20020091914 A1	☐	Multi-threading techniques for a processor utilizing a replay queue	712/219
55	US 20020087849 A1	☐	Full multiprocessor speculation mechanism in a symmetric multiprocessor (smp) System	712/235
56	US 20020087833 A1	☐	Method and apparatus for distributed processor dispersal logic	712/215
57	US 20020087827 A1	☐	Architecture of psm-mpus and coprocessors	712/22
58	US 20020083398 A1	☐	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
59	US 20020083303 A1	☐	Program-controlled unit	712/215
60	US 20020083300 A1	☐	System and method for register renaming	712/203
61	US 20020078285 A1	☐	Reduction of interrupts in remote procedure calls	710/260
62	US 20020073255 A1	☐	Hierarchical selection of direct and indirect counting events in a performance monitor unit	710/104
63	US 20020066005 A1	☐	Data processor with an improved data dependence detector	712/218
64	US 20020062435 A1	☐	PRIORITIZED INSTRUCTION SCHEDULING FOR MULTI-STREAMING PROCESSORS	712/7
65	US 20020046325 A1	☐	Buffer memory management in a system having multiple execution entities	711/122
66	US 20020038415 A1	☐	Processor architecture with independently addressable memory banks for storing instructions to be executed	712/206
67	US 20020032827 A1	☐	STRUCTURE AND METHOD FOR PROVIDING MULTIPLE EXTERNALLY ACCESSIBLE ON-CHIP CACHES IN A MICROPROCESSOR	711/3
68	US 20020029328 A1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23

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69	US 20020016903 A1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
70	US 20020013915 A1	☐	Data processing control system, controller, data processing control method, program, and medium	714/6
71	US 20020007450 A1	☐	Line-oriented reorder buffer	712/23
72	US 20010054141 A1	☐	Microsequencer with nested loop counters	712/241
73	US 20010054140 A1	☐	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
74	US 20010054138 A1	☐	Instruction buffer and buffer queue control method	712/215
75	US 20010054137 A1	☐	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11
76	US 20010052055 A1	☐	Active window management for reorder buffer	711/147
77	US 20010051969 A1	☐	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/514
78	US 20010049770 A1	☐	BUFFER MEMORY MANAGEMENT IN A SYSTEM HAVING MULTIPLE EXECUTION ENTITIES	711/129
79	US 20010044912 A1	☐	Reliable hardware support for the use of formal languages in high assurance systems	714/30
80	US 20010042192 A1	☐	Mechanism for self-initiated instruction issuing and method therefor	712/215
81	US 20010032307 A1	☐	MICRO-INSTRUCTION QUEUE FOR A MICROPROCESSOR INSTRUCTION PIPELINE	712/219
82	US 20010032305 A1	☐	Methods and apparatus for dual-use coprocessing/debug interface	712/34
83	US 20010030943 A1	☐	System of controlling the flow of information between senders and receivers across links being used as channels	370/231
84	US 20010029590 A1	☐	Processor having execution core sections operating at different clock rates	713/501
85	US 20010025317 A1	☐	Method of controlling the flow of information between senders and receivers across links being used as channels	709/237

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86	US 20010025237 A1	☐	Computer system with debug facility	703/26
87	US 20010023425 A1	☐	Method and apparatus for rounding in a multiplier arithmetic	708/620
88	US 20010018735 A1	☐	Data processor and data processing system	712/207
89	US 20010016899 A1	☐	Data-processing device	712/215
90	US 20010014941 A1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
91	US 20010011343 A1	☐	System and method for register renaming	712/217
92	US 20010010073 A1	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/218
93	US 20010010062 A1	☐	Data processing system and microcomputer	710/113
94	US 20010010051 A1	☐	Method and apparatus for multi-function arithmetic	708/502
95	US 6549985 B1	☐	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/123
96	US 6543028 B1	☐	Silent data corruption prevention due to instruction corruption by soft errors	714/800
97	US 6542986 B1	☐	Resolving dependencies among concurrently dispatched instructions in a superscalar microprocessor	712/217
98	US 6542984 B1	☐	Scheduler capable of issuing and reissuing dependency chains	712/214
99	US 6542982 B2	☐	Data processer and data processing system	712/207
100	US 6539469 B1	☐	Rotator circular buffer with entries to store divided bundles of instructions from each cache line for optimized instruction supply	712/205
101	US 6535905 B1	☐	Method and apparatus for thread switching within a multithreaded processor	718/108
102	US 6526421 B1	☐	Method of scheduling garbage collection	707/206
103	US 6523110 B1	☐	Decoupled fetch-execute engine with static branch prediction support	712/239
104	US 6513107 B1	☐	Vector transfer system generating address error exception when vector to be transferred does not start and end on same memory page	712/4
105	US 6505295 B1	☐	Data processor	712/241

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106	US 6504895 B2	☐	Method and system monitoring image detection	378/19
107	US 6499100 B1	☐	Enhanced instruction decoding	712/210
108	US 6496924 B2	☐	Data processing apparatus including a plurality of pipeline processing mechanisms in which memory access instructions are carried out in a memory access pipeline	712/216
109	US 6493820 B2	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
110	US 6493774 B2	☐	Data processing system and microcomputer	710/100
111	US 6490673 B1	☐	Processor, compiling apparatus, and compile program recorded on a recording medium	712/213
112	US 6487675 B2	☐	Processor having execution core sections operating at different clock rates	713/501
113	US 6477639 B1	☐	Branch instruction mechanism for processor	712/237
114	US 6477599 B1	☐	Data processing system and microcomputer	710/241
115	US 6475762 B2	☐	Prioritized instruction scheduling for multi-streaming processors	718/108
116	US 6473850 B1	☐	System and method for handling instructions occurring after an ISYNC instruction	712/244
117	US 6470422 B2	☐	Buffer memory management in a system having multiple execution entities	711/129
118	US 6463524 B1	☐	Superscalar processor and method for incrementally issuing store instructions	712/221
119	US 6463523 B1	☐	Method and apparatus for delaying the execution of dependent loads	712/216
120	US 6463522 B1	☐	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
121	US 6460130 B1	☐	Detecting full conditions in a queue	712/32
122	US 6460129 B1	☐	Pipeline operation method and pipeline operation device to interlock the translation of instructions based on the operation of a non-pipeline operation unit	712/31
123	US 6453412 B1	☐	Method and apparatus for reissuing paired MMX instructions singly during exception handling	712/244
124	US 6453405 B1	☐	Microprocessor with non-aligned circular addressing	711/201
125	US 6449710 B1	☐	Stitching parcels	712/216
126	US 6446197 B1	☐	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
127	US 6446164 B1	☐	Test mode accessing of an internal cache memory	711/118
128	US 6442627 B1	☐	Output FIFO data transfer control device	710/52

	Document ID	U	Title	Current OR
129	US 6442613 B1	☐	Controlling the flow of information between senders and receivers across links being used as channels	709/232
130	US 6438673 B1	☐	Correlated address prediction	711/213
131	US 6434693 B1	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/245
132	US 6434691 B1	☐	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
133	US 6427188 B1	☐	Method and system for early tag accesses for lower-level caches in parallel with first-level cache	711/122
134	US 6421696 B1	☐	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
135	US 6412064 B1	☐	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
136	US 6408375 B2	☐	System and method for register renaming	712/23
137	US 6401190 B1	☐	Parallel computing units having special registers storing large bit widths	712/24
138	US 6397239 B2	☐	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/505
139	US 6397238 B2	☐	Method and apparatus for rounding in a multiplier	708/497
140	US 6393554 B1	☐	Method and apparatus for performing vector and scalar multiplication and calculating rounded products	712/221
141	US 6393549 B1	☐	Instruction alignment unit for routing variable byte-length instructions	712/204
142	US 6393446 B1	☐	32-bit and 64-bit dual mode rotator	708/209
143	US 6389531 B1	☐	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
144	US 6389512 B1	☐	Microprocessor configured to detect updates to instructions outstanding within an instruction processing pipeline and computer system including same	711/125
145	US 6389451 B1	☐	Distributed digital rule processor for single system image on a clustered network and method	709/201
146	US 6385715 B1	☐	Multi-threading for a processor utilizing a replay queue	712/219
147	US 6381689 B2	☐	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
148	US 6381625 B2	☐	Method and apparatus for calculating a power of an operand	708/606
149	US 6374348 B1	☐	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
150	US 6367067 B1	☐	Program conversion apparatus for constant reconstructing VLIW processor	717/154

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151	US 6363475 B1	☐	Apparatus and method for program level parallelism in a VLIW processor	712/206
152	US 6360317 B1	☐	Predecoding multiple instructions as one combined instruction and detecting branch to one of the instructions	712/233
153	US 6360315 B1	☐	Method and apparatus that supports multiple assignment code	712/219
154	US 6360311 B1	☐	Processor architecture with independently addressable memory banks for storing instructions to be executed	712/206
155	US 6356997 B1	☐	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
156	US 6356928 B1	☐	Method for partitioning tasks into stateless elements	718/101
157	US 6356918 B1	☐	Method and system for managing registers in a data processing system supports out-of-order and speculative instruction execution	707/203
158	US 6351805 B1	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
159	US 6351802 B1	☐	Method and apparatus for constructing a pre-scheduled instruction cache	712/215
160	US 6343288 B1	☐	Single pass space efficient system and method for generating an approximate quantile in a data set having an unknown size	707/7
161	US 6336154 B1	☐	Method of operating a computer system by identifying source code computational elements in main memory	710/35
162	US 6334184 B1	☐	Processor and method of fetching an instruction that select one of a plurality of decoded fetch addresses generated in parallel to form a memory request	712/235
163	US 6330661 B1	☐	Reducing inherited logical to physical register mapping information between tasks in multithread system using register group identifier	712/228
164	US 6330657 B1	☐	Pairing of micro instructions in the instruction queue	712/23
165	US 6324643 B1	☐	Branch prediction and target instruction control for processor	712/237
166	US 6324640 B1	☐	System and method for dispatching groups of instructions using pipelined register renaming	712/217
167	US 6324639 B1	☐	Instruction converting apparatus using parallel execution code	712/212
168	US 6314502 B1	☐	Method and apparatus for opportunistic queue processing	711/162
169	US 6311261 B1	☐	Apparatus and method for improving superscalar processors	712/23
170	US 6308260 B1	☐	Mechanism for self-initiated instruction issuing and method therefor	712/215
171	US 6308259 B1	☐	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
172	US 6304953 B1	☐	Computer processor with instruction-specific schedulers	712/215
173	US 6302698 B1	☐	Method and apparatus for on-line teaching and learning	434/323

	Document ID	U	Title	Current OR
174	US 6298367 B1	☐	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/524
175	US 6295601 B1	☐	System and method using partial trap barrier instruction to provide trap barrier class-based selective stall of instruction processing pipeline	712/244
176	US 6295600 B1	☐	Thread switch on blocked load or store using instruction thread field	712/228
177	US 6292845 B1	☐	Processing unit having independent execution units for parallel execution of instructions of different category with instructions having specific bits indicating instruction size and category respectively	710/5
178	US 6289437 B1	☐	Data processing system and method for implementing an efficient out-of-order issue mechanism	712/217
179	US 6282630 B1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
180	US 6279105 B1	☐	Pipelined two-cycle branch target address cache	712/238
181	US 6279101 B1	☐	Instruction decoder/dispatch	712/215
182	US 6279100 B1	☐	Local stall control method and structure in a microprocessor	712/24
183	US 6272619 B1	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
184	US 6272617 B1	☐	System and method for register renaming	712/23
185	US 6269440 B1	☐	Accelerating vector processing using plural sequencers to process multiple loop iterations simultaneously	712/241
186	US 6269384 B1	☐	Method and apparatus for rounding and normalizing results within a multiplier	708/497
187	US 6266761 B1	☐	Method and system in an information processing system for efficient maintenance of copies of values stored within registers	712/23
188	US 6260138 B1	☐	Method and apparatus for branch instruction processing in a processor	712/239
189	US 6260135 B1	☐	Parallel processing unit and instruction issuing system	712/214
190	US 6256745 B1	☐	Processor having execution core sections operating at different clock rates	713/501
191	US 6256720 B1	☐	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
192	US 6256653 B1	☐	Multi-function bipartite look-up table	708/290
193	US 6250821 B1	☐	Method and apparatus for processing branch instructions in an instruction buffer	712/238
194	US 6249862 B1	☐	Dependency table for reducing dependency checking hardware	712/218
195	US 6247124 B1	☐	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240

	Document ID	U	Title	Current OR
196	US 6247121 B1	☐	Multithreading processor with thread predictor	712/239
197	US 6247120 B1	☐	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
198	US 6247115 B1	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
199	US 6247114 B1	☐	Rapid selection of oldest eligible entry in a queue	712/216
200	US 6247064 B1	☐	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	13601	execut$3 near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	USPAT; US-PGPUB
3	L5	1850	1 near30 ((select$3 multiplex$3 rout$3 switch$3 crossbar bar) near10 instruction)	USPAT; US-PGPUB
4	L6	65	5 near99 3	USPAT; US-PGPUB
5	L7	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L8	398	7 near30 ((select$3 multiplex$3 rout$3 switch$3 crossbar bar) near10 instruction)	EPO; JPO; DERWENT; IBM_TDB
7	L9	3446	execut$3 near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	EPO; JPO; DERWENT; IBM_TDB
8	L10	37	8 and 9	EPO; JPO; DERWENT; IBM_TDB
9	L18	225	5 near20 ((process$3 function$3 execut$3) adj2 (unit element module)) not 6	USPAT; US-PGPUB
10	L19	830	3 and 5 not (6 18)	USPAT; US-PGPUB
11	L20	220	((queue buffer fifo) near5 instruction).ab,ti. and 19	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040039952 A1	☐	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
2	US 20040030866 A1	☐	Apparatus and method for buffering instructions and late-generated related information using history of previous load/shifts	712/217
3	US 20040030865 A1	☐	Method and apparatus for implementing two architectures in a chip	712/209
4	US 20040003203 A1	☐	Instruction fetch control device and instruction fetch control method	712/205
5	US 20040003202 A1	☐	Instruction fetch control apparatus	712/205
6	US 20030212726 A1	☐	Floating point unit power reduction scheme	708/501
7	US 20030163679 A1	☐	Method and apparatus for loop buffering digital signal processing instructions	712/241
8	US 20030154358 A1	☐	Apparatus and method for dispatching very long instruction word having variable length	712/24
9	US 20030135719 A1	☐	Method and system using hardware assistance for tracing instruction disposition information	712/227
10	US 20030135718 A1	☐	Method and system using hardware assistance for instruction tracing by revealing executed opcode or instruction	712/227
11	US 20030120898 A1	☐	Method and circuits for early detection of a full queue	712/205
12	US 20030084273 A1	☐	Processor and method of testing a processor for hardware faults utilizing a pipeline interlocking test instruction	712/227
13	US 20030061466 A1	☐	Method and apparatus for fast dependency cooridnate matching	712/217
14	US 20030056134 A1	☐	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
15	US 20030009622 A1	☐	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/118
16	US 20030005262 A1	☐	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
17	US 20030004683 A1	☐	Instruction pre-fetching mechanism for a multithreaded program execution	702/186

	Document ID	U	Title	Current OR
18	US 20020161987 A1	☐	System and method including distributed instruction buffers holding a second instruction form	712/205
19	US 20020120829 A1	☐	Data processer and data processing system	712/207
20	US 20020103971 A1	☐	Control circuit for cache system and method of controlling cache system	711/118
21	US 20020091914 A1	☐	Multi-threading techniques for a processor utilizing a replay queue	712/219
22	US 20020087832 A1	☐	Instruction fetch apparatus for wide issue processors and method of operation	712/206
23	US 20020083302 A1	☐	Hardware instruction translation within a processor pipeline	712/209
24	US 20020007450 A1	☐	Line-oriented reorder buffer	712/23
25	US 20010037444 A1	☐	INSTRUCTION BUFFERING MECHANISM	712/207
26	US 20010018735 A1	☐	Data processor and data processing system	712/207
27	US 20010016899 A1	☐	Data-processing device	712/215
28	US 6704856 B1	☐	Method for compacting an instruction queue	712/215
29	US 6701426 B1	☐	Switching between a plurality of branch prediction processes based on which instruction set is operational wherein branch history data structures are the same for the plurality of instruction sets	712/239
30	US 6691221 B2	☐	Loading previously dispatched slots in multiple instruction dispatch buffer before dispatching remaining slots for parallel execution	712/215
31	US 6687857 B1	☐	Microcomputer which can execute a monitor program supplied from a debugging tool	714/38
32	US 6662297 B1	☐	Allocation of processor bandwidth by inserting interrupt servicing instructions to intervene main program in instruction queue mechanism	712/245
33	US 6636883 B1	☐	Mechanism for passing information between queuing and de-queuing processes	718/102
34	US 6618801 B1	☐	Method and apparatus for implementing two architectures in a chip using bundles that contain microinstructions and template information	712/215
35	US 6609201 B1	☐	Secure program execution using instruction buffer interdependencies	713/187
36	US 6609191 B1	☐	Method and apparatus for speculative microinstruction pairing	712/216

	Document ID	U	Title	Current OR
37	US 6604191 B1	☐	Method and apparatus for accelerating instruction fetching for a processor	712/207
38	US 6598155 B1	☐	Method and apparatus for loop buffering digital signal processing instructions	712/241
39	US 6571329 B1	☐	Detection of overwrite modification by preceding instruction possibility of fetched instruction code using fetched instructions counter and store target address	712/205
40	US 6553484 B1	☐	Instruction-issuing circuit that sets reference dependency information in a preceding instruction when a succeeding instruction is stored in an instruction out-of-order buffer	712/217
41	US 6553482 B1	☐	Universal dependency vector/queue entry	712/216
42	US 6550003 B1	☐	Not reported jump buffer	712/218
43	US 6549985 B1	☐	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/123
44	US 6542987 B1	☐	Method and circuits for early detection of a full queue	712/217
45	US 6542982 B2	☐	Data processer and data processing system	712/207
46	US 6539469 B1	☐	Rotator circular buffer with entries to store divided bundles of instructions from each cache line for optimized instruction supply	712/205
47	US 6530013 B1	☐	Instruction control apparatus for loading plurality of instructions into execution stage	712/206
48	US 6477640 B1	☐	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
49	US 6470443 B1	☐	Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information	712/205
50	US 6463524 B1	☐	Superscalar processor and method for incrementally issuing store instructions	712/221
51	US 6460130 B1	☐	Detecting full conditions in a queue	712/32
52	US 6442707 B1	☐	Alternate fault handler	714/10
53	US 6442681 B1	☐	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
54	US 6434691 B1	☐	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
55	US 6393536 B1	☐	Load/store unit employing last-in-buffer indication for rapid load-hit-store	711/159
56	US 6389531 B1	☐	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
57	US 6385715 B1	☐	Multi-threading for a processor utilizing a replay queue	712/219
58	US 6381689 B2	☐	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215

	Document ID	U	Title	Current OR
59	US 6374348 B1	☐	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
60	US 6367006 B1	☐	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
61	US 6351802 B1	☐	Method and apparatus for constructing a pre-scheduled instruction cache	712/215
62	US 6341347 B1	☐	Thread switch logic in a multiple-thread processor	712/228
63	US 6338133 B1	☐	Measured, allocation of speculative branch instructions to processor execution units	712/214
64	US 6321325 B1	☐	Dual in-line buffers for an instruction fetch unit	712/204
65	US 6321310 B1	☐	Memory architecture for a computer system	711/154
66	US 6314509 B1	☐	Efficient method for fetching instructions having a non-power of two size	712/204
67	US 6311261 B1	☐	Apparatus and method for improving superscalar processors	712/23
68	US 6308259 B1	☐	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
69	US 6292884 B1	☐	Reorder buffer employing last in line indication	712/216
70	US 6292882 B1	☐	Method and apparatus for filtering valid information for downstream processing	712/204
71	US 6292845 B1	☐	Processing unit having independent execution units for parallel execution of instructions of different category with instructions having specific bits indicating instruction size and category respectively	710/5
72	US 6289437 B1	☐	Data processing system and method for implementing an efficient out-of-order issue mechanism	712/217
73	US 6272620 B1	☐	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
74	US 6253305 B1	☐	Microprocessor for supporting reduction of program codes in size	712/32
75	US 6249862 B1	☐	Dependency table for reducing dependency checking hardware	712/218
76	US 6247114 B1	☐	Rapid selection of oldest eligible entry in a queue	712/216
77	US 6240508 B1	☐	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
78	US 6240507 B1	☐	Mechanism for multiple register renaming and method therefor	712/217
79	US 6237082 B1	☐	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
80	US 6237079 B1	☐	Coprocessor interface having pending instructions queue and clean-up queue and dynamically allocating memory	712/34

	Document ID	U	Title	Current OR
81	US 6216200 B1	☐	Address queue	711/100
82	US 6212623 B1	☐	Universal dependency vector/queue entry	712/216
83	US 6209084 B1	☐	Dependency table for reducing dependency checking hardware	712/233
84	US 6192465 B1	☐	Using multiple decoders and a reorder queue to decode instructions out of order	712/212
85	US 6192461 B1	☐	Method and apparatus for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle	712/23
86	US 6189092 B1	☐	Pipeline processor capable of reducing branch hazards with small-scale circuit	712/241
87	US 6189089 B1	☐	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
88	US 6189087 B1	☐	Superscalar instruction decoder including an instruction queue	712/208
89	US 6185672 B1	☐	Method and apparatus for instruction queue compression	712/217
90	US 6178497 B1	☐	System and method for determining the relative age of instructions in a processor	712/214
91	US 6175897 B1	☐	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
92	US 6157998 A	☐	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
93	US 6142683 A	☐	Debug interface including data steering between a processor, an input/output port, and a trace logic	717/128
94	US 6141742 A	☐	Method for reducing number of bits used in storage of instruction address pointer values	711/220
95	US 6134651 A	☐	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
96	US 6128722 A	☐	Data processing system having an apparatus for exception tracking during out-of-order operation and method therefor	712/23
97	US 6122729 A	☐	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
98	US 6122727 A	☐	Symmetrical instructions queue for high clock frequency scheduling	712/214
99	US 6122724 A	☐	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
100	US 6119220 A	☐	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
101	US 6115807 A	☐	Static instruction decoder utilizing a circular queue to decode instructions and select instructions to be issued	712/212
102	US 6112019 A	☐	Distributed instruction queue	712/214

	Document ID	U	Title	Current OR
103	US 6108775 A	☐	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
104	US 6108769 A	☐	Dependency table for reducing dependency checking hardware	712/216
105	US 6085311 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
106	US 6085297 A	☐	Single-chip memory system including buffer	711/158
107	US 6073159 A	☐	Thread properties attribute vector based thread selection in multithreading processor	718/103
108	US 6065112 A	☐	Microprocessor with arithmetic processing units and arithmetic execution unit	712/221
109	US 6065110 A	☐	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
110	US 6052708 A	☐	Performance monitoring of thread switch events in a multithreaded processor	718/108
111	US 6032251 A	☐	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
112	US 6026482 A	☐	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
113	US 6021488 A	☐	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
114	US 5960071 A	☐	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
115	US 5833842 A	☐	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
116	US 5742740 A	☐	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
117	US 5961634 A	☐	Reorder buffer having a future file for storing speculative instruction execution results	712/218
118	US 5960467 A	☐	Apparatus for efficiently providing memory operands for instructions	711/214
119	US 5958043 A	☐	Superscalar processor with forward map buffer in multiple instruction parallel issue/execution management system	712/216
120	US 5951675 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/215
121	US 5946468 A	☐	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
122	US 5944811 A	☐	Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies	712/23
123	US 5935241 A	☐	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
124	US 5930520 A	☐	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	712/23
125	US 5923862 A	☐	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208

	Document ID	U	Title	Current OR
126	US 5915110 A	☐	Branch misprediction recovery in a reorder buffer having a future file	712/239
127	US 5913059 A	☐	Multi-processor system for inheriting contents of register from parent thread to child thread	718/104
128	US 5903740 A	☐	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
129	US 5896518 A	☐	Instruction queue scanning using opcode identification	712/208
130	US 5887185 A	☐	Interface for coupling a floating point unit to a reorder buffer	712/23
131	US 5887161 A	☐	Issuing instructions in a processor supporting out-of-order execution	712/244
132	US 5887152 A	☐	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
133	US 5872951 A	☐	Reorder buffer having a future file for storing speculative instruction execution results	712/218
134	US 5872946 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
135	US 5867698 A	☐	Apparatus and method for accessing a branch target buffer	712/238
136	US 5864690 A	☐	Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue	712/208
137	US 5859992 A	☐	Instruction alignment using a dispatch list and a latch list	712/204
138	US 5850542 A	☐	Microprocessor instruction hedge-fetching in a multiprediction branch environment	712/235
139	US 5848269 A	☐	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
140	US 5845101 A	☐	Prefetch buffer for storing instructions prior to placing the instructions in an instruction cache	712/207
141	US 5845100 A	☐	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
142	US 5835968 A	☐	Apparatus for providing memory and register operands concurrently to functional units	711/214
143	US 5829021 A	☐	System for controlling operating timing of a cache memory	711/118
144	US 5826096 A	☐	Minimal instruction set computer architecture and multiple instruction issue method	712/24
145	US 5822574 A	☐	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
146	US 5822555 A	☐	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
147	US 5819056 A	☐	Instruction buffer organization method and system	712/204
148	US 5805878 A	☐	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239

	Document ID	U	Title	Current OR
149	US 5805853 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
150	US 5805852 A	☐	Parallel processor performing bypass control by grasping portions in which instructions exist	712/218
151	US 5796998 A	☐	Apparatus and method for performing branch target address calculation and branch prediciton in parallel in an information handling system	712/239
152	US 5778246 A	☐	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
153	US 5768555 A	☐	Reorder buffer employing last in buffer and last in line bits	712/216
154	US 5765220 A	☐	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
155	US 5764970 A	☐	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
156	US 5764938 A	☐	Resynchronization of a superscalar processor	712/200
157	US 5754813 A	☐	Data processor	712/216
158	US 5748978 A	☐	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
159	US 5742781 A	☐	Decoded instruction buffer apparatus and method for reducing power consumption in a digital signal processor	712/208
160	US 5721857 A	☐	Method and apparatus for saving the effective address of floating point memory operations in an out-of-order microprocessor	712/23
161	US 5706492 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/238
162	US 5699537 A	☐	Processor microarchitecture for efficient dynamic scheduling and execution of chains of dependent instructions	712/217
163	US 5680597 A	☐	System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions	712/226
164	US 5680565 A	☐	Method and apparatus for performing page table walks in a microprocessor capable of processing speculative instructions	711/205
165	US 5649225 A	☐	Resynchronization of a superscalar processor	712/23
166	US 5632023 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
167	US 5630082 A	☐	Apparatus and method for instruction queue scanning	712/213
168	US 5623615 A	☐	Circuit and method for reducing prefetch cycles on microprocessors	712/238
169	US 5619730 A	☐	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	710/35
170	US 5619667 A	☐	Method and apparatus for fast fill of translator instruction queue	712/208

	Document ID	U	Title	Current OR
171	US 5619663 A	☐	Computer instruction prefetch system	712/207
172	US 5608885 A	☐	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
173	US 5602998 A	☐	Dequeue instruction in a system architecture for improved message passing and process synchronization	712/225
174	US 5600806 A	☐	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
175	US 5598544 A	☐	Instruction buffer device for processing an instruction set of variable-length instruction codes	712/204
176	US 5586277 A	☐	Method for parallel steering of fixed length fields containing a variable length instruction from an instruction buffer to parallel decoders	712/210
177	US 5574871 A	☐	Method and apparatus for implementing a set-associative branch target buffer	712/200
178	US 5564041 A	☐	Microprocessor for inserting a bus cycle in an instruction set to output an internal information for an emulation	703/23
179	US 5553254 A	☐	Instruction cache access and prefetch process controlled by a predicted instruction-path mechanism	712/207
180	US 5542058 A	☐	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
181	US 5537559 A	☐	Exception handling circuit and method	712/244
182	US 5509130 A	☐	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
183	US 5500948 A	☐	Translating instruction pointer virtual addresses to physical addresses for accessing an instruction cache	711/205
184	US 5481743 A	☐	Minimal instruction set computer architecture and multiple instruction issue method	712/23
185	US 5467473 A	☐	Out of order instruction load and store comparison	712/23
186	US 5448705 A	☐	RISC microprocessor architecture implementing fast trap and exception state	712/244
187	US 5423016 A	☐	Block buffer for instruction/operand caches	711/123
188	US 5371864 A	☐	Apparatus for concurrent multiple instruction decode in variable length instruction set computer	712/206
189	US 5317701 A	☐	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
190	US 5265213 A	☐	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
191	US 5263169 A	☐	Bus arbitration and resource management for concurrent vector signal processor architecture	712/7
192	US 5197145 A	☐	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143

	Document ID	U	Title	Current OR
193	US 5197131 A	☐	Instruction buffer system for switching execution of current instruction to a branch or to a return from subroutine	712/238
194	US 5170474 A	☐	Method of searching a queue in response to a search instruction	707/6
195	US 5148528 A	☐	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
196	US 5142633 A	☐	Preprocessing implied specifiers in a pipelined processor	712/225
197	US 5119495 A	☐	Minimizing hardware pipeline breaks using software scheduling techniques during compilation	717/153
198	US 5113515 A	☐	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
199	US 5101341 A	☐	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
200	US 5081698 A	☐	Method and apparatus for graphics display data manipulation	345/422

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu$3 dispatch$3 schedul$3 execut$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent$3 simultaneous$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 6247124 B1	☐	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
2	US 6247121 B1	☐	Multithreading processor with thread predictor	712/239
3	US 6247120 B1	☐	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
4	US 6247115 B1	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
5	US 6247114 B1	☐	Rapid selection of oldest eligible entry in a queue	712/216
6	US 6247064 B1	☐	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312
7	US 6243836 B1	☐	Apparatus and method for circular buffering on an on-chip discontinuity trace	714/45
8	US 6240509 B1	☐	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
9	US 6240508 B1	☐	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
10	US 6237083 B1	☐	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
11	US 6237082 B1	☐	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
12	US 6230254 B1	☐	System and method for handling load and/or store operators in a superscalar microprocessor	712/23
13	US 6226641 B1	☐	Access control for groups of related data items	707/8
14	US 6223198 B1	☐	Method and apparatus for multi-function arithmetic	708/620
15	US 6223192 B1	☐	Bipartite look-up table with output values having minimized absolute error	708/270
16	US 6216234 B1	☐	Processor having execution core sections operating at different clock rates	713/501
17	US 6209084 B1	☐	Dependency table for reducing dependency checking hardware	712/233
18	US 6209082 B1	☐	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
19	US 6209081 B1	☐	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system	712/215
20	US 6205542 B1	☐	Processor pipeline including replay	712/219
21	US 6192468 B1	☐	Apparatus and method for detecting microbranches early	712/231
22	US 6192466 B1	☐	Pipeline control for high-frequency pipelined designs	712/214

	Document ID	U	Title	Current OR
23	US 6192461 B1	☐	Method and apparatus for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle	712/23
24	US 6189089 B1	☐	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
25	US 6185672 B1	☐	Method and apparatus for instruction queue compression	712/217
26	US 6182210 B1	☐	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
27	US 6175910 B1	☐	Speculative instructions exection in VLIW processors	712/217
28	US 6170051 B1	☐	Apparatus and method for program level parallelism in a VLIW processor	712/225
29	US 6167507 A	☐	Apparatus and method for floating point exchange dispatch with reduced latency	712/213
30	US 6167503 A	☐	Register and instruction controller for superscalar processor	712/23
31	US 6163839 A	☐	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
32	US 6163821 A	☐	Method and apparatus for balancing load vs. store access to a primary data cache	710/57
33	US 6161172 A	☐	Method for concurrently dispatching microcode and directly-decoded instructions in a microprocessor	712/204
34	US 6157988 A	☐	Method and apparatus for high performance branching in pipelined microsystems	711/140
35	US 6154765 A	☐	Distributed digital rule processor for single system image on a clustered network and method	709/201
36	US 6148395 A	☐	Shared floating-point unit in a single chip multiprocessor	712/222
37	US 6144982 A	☐	Pipeline processor and computing system including an apparatus for tracking pipeline resources	718/104
38	US 6144980 A	☐	Method and apparatus for performing multiple types of multiplication including signed and unsigned multiplication	708/627
39	US 6142683 A	☐	Debug interface including data steering between a processor, an input/output port, and a trace logic	717/128
40	US 6141740 A	☐	Apparatus and method for microcode patching for generating a next address	711/215
41	US 6138231 A	☐	System and method for register renaming	712/216
42	US 6134651 A	☐	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
43	US 6134645 A	☐	Instruction completion logic distributed among execution units for improving completion efficiency	712/23
44	US 6134574 A	☐	Method and apparatus for achieving higher frequencies of exactly rounded results	708/551

	Document ID	U	Title	Current OR
45	US 6131157 A	☐	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
46	US 6131155 A	☐	Programmer-visible uncached load/store unit having burst capability	712/207
47	US 6131104 A	☐	Floating point addition pipeline configured to perform floating point-to-integer and integer-to-floating point conversion operations	708/204
48	US 6128723 A	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
49	US 6128710 A	☐	Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system	711/152
50	US 6125443 A	☐	Interrupt processing system and method for information processing system of pipeline control type	712/244
51	US 6115733 A	☐	Method and apparatus for calculating reciprocals and reciprocal square roots	708/654
52	US 6115732 A	☐	Method and apparatus for compressing intermediate products	708/625
53	US 6115730 A	☐	Reloadable floating point unit	708/505
54	US 6112317 A	☐	Processor performance counter for sampling the execution frequency of individual instructions	714/47
55	US 6112019 A	☐	Distributed instruction queue	712/214
56	US 6108769 A	☐	Dependency table for reducing dependency checking hardware	712/216
57	US 6108766 A	☐	Structure of processor having a plurality of main processors and sub processors, and a method for sharing the sub processors	712/34
58	US 6106573 A	☐	Apparatus and method for tracing microprocessor instructions	717/128
59	US 6105128 A	☐	Method and apparatus for dispatching instructions to execution units in waves	712/215
60	US 6101597 A	☐	Method and apparatus for maximum throughput scheduling of dependent operations in a pipelined processor	712/218
61	US 6101594 A	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
62	US 6098168 A	☐	System for completing instruction out-of-order which performs target address comparisons prior to dispatch	712/218
63	US 6098167 A	☐	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
64	US 6094668 A	☐	Floating point arithmetic unit including an efficient close data path	708/505
65	US 6092181 A	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
66	US 6088790 A	☐	Using a table to track and locate the latest copy of an operand	712/218

	Document ID	U	Title	Current OR
67	US 6088715 A	☐	Close path selection unit for performing effective subtraction within a floating point arithmetic unit	708/505
68	US 6085311 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
69	US 6085213 A	☐	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and summing the products	708/603
70	US 6085212 A	☐	Efficient method for performing close path subtraction in a floating point arithmetic unit	708/505
71	US 6085208 A	☐	Leading one prediction unit for normalizing close path subtraction results within a floating point arithmetic unit	708/205
72	US 6081887 A	☐	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
73	US 6078270 A	☐	Data transmission method of a remote controller	340/825.72
74	US 6076153 A	☐	Processor pipeline including partial replay	712/23
75	US 6073217 A	☐	Method for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
76	US 6065112 A	☐	Microprocessor with arithmetic processing units and arithmetic execution unit	712/221
77	US 6065110 A	☐	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
78	US 6055650 A	☐	Processor configured to detect program phase changes and to adapt thereto	714/39
79	US 6052776 A	☐	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
80	US 6052708 A	☐	Performance monitoring of thread switch events in a multithreaded processor	718/108
81	US 5849863 A	☐	Predecoding technique for indicating locations of opcode bytes in variable byte-length instructions within a superscalar microprocessor	712/213
82	US 5847370 A	☐	Control of processor pipeline movement through replay queue and pointer backup	712/219
83	US 5844450 A	☐	Processor for VLIW instruction	712/24
84	US 5842022 A	☐	System, method, and program product for loop instruction scheduling hardware lookahead	717/156
85	US 5841398 A	☐	Massively parallel multiple-folded clustered processor mesh array	712/11
86	US 5838954 A	☐	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
87	US 5838953 A	☐	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
88	US 5838383 A	☐	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and calculating a rounded products	708/628
89	US 5835394 A	☐	System for providing high performance speculative processing of complex load/store instructions by generating primitive instructions in the load/store unit and sequencer in parallel	712/245

	Document ID	U	Title	Current OR
90	US 6035389 A	☐	Scheduling instructions with different latencies	712/216
91	US 6032252 A	☐	Apparatus and method for efficient loop control in a superscalar microprocessor	712/233
92	US 6029244 A	☐	Microprocessor including an efficient implementation of extreme value instructions	712/223
93	US 6026483 A	☐	Method and apparatus for simultaneously performing arithmetic on two or more pairs of operands	712/221
94	US 6026482 A	☐	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
95	US 6023756 A	☐	Instruction processing method and system for variable-length instructions	712/208
96	US 6021488 A	☐	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
97	US 6021485 A	☐	Forwarding store instruction result to load instruction with reduced stall or flushing by effective/real data address bytes matching	712/216
98	US 6021484 A	☐	Dual instruction set architecture	712/41
99	US 6016541 A	☐	Instruction controlling system and method thereof	712/217
100	US 6014741 A	☐	Apparatus and method for predicting an end of a microcode loop	712/233
101	US 6012141 A	☐	Apparatus for detecting and executing traps in a superscalar processor	712/244
102	US 6009514 A	☐	Computer method and apparatus for analyzing program instructions executing in a computer system	712/236
103	US 6009513 A	☐	Apparatus and method for detecting microbranches early	712/231
104	US 6006324 A	☐	High performance superscalar alignment unit	712/204
105	US 6006318 A	☐	General purpose, dynamic partitioning, programmable media processor	712/28
106	US 5960485 A	☐	Concurrent execution of machine context synchronization operations and non-interruptible instructions	713/400
107	US 5960462 A	☐	Method and apparatus for controlling an instruction pipeline in a data processing system	712/215
108	US 5957943 A	☐	Method and system for interrupt handling during emulation in a data processing system	703/21
109	US 5875995 A	☐	Method and apparatus for predicting when load instructions can be executed out-of order	712/216
110	US 5875993 A	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/206
111	US 5875885 A	☐	One-chip microprocessor with error detection on the chip	712/1
112	US 5983343 A	☐	Data processing system having an apparatus for de-serialized status register operation and method therefor	712/237

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113	US 5983342 A	☐	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
114	US 5983341 A	☐	Data processing system and method for extending the time for execution of an instruction	712/216
115	US 5983337 A	☐	Apparatus and method for patching an instruction by providing a substitute instruction or instructions from an external memory responsive to detecting an opcode of the instruction	712/32
116	US 5978908 A	☐	Computer instruction supply	712/240
117	US 5978896 A	☐	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23
118	US 5974531 A	☐	Methods and systems of stack renaming for superscalar stack-based data processors	712/202
119	US 5974522 A	☐	Machine for processing interrupted out-of-order instructions	712/23
120	US 5974240 A	☐	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
121	US 5968135 A	☐	Processing instructions up to load instruction after executing sync flag monitor instruction during plural processor shared memory store/load access synchronization	709/400
122	US 5966544 A	☐	Data speculatable processor having reply architecture	712/32
123	US 5964868 A	☐	Method and apparatus for implementing a speculative return stack buffer	712/234
124	US 5963723 A	☐	System for pairing dependent instructions having non-contiguous addresses during dispatch	712/215
125	US 5961636 A	☐	Checkpoint table for selective instruction flushing in a speculative execution unit	712/228
126	US 5961634 A	☐	Reorder buffer having a future file for storing speculative instruction execution results	712/218
127	US 5961629 A	☐	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
128	US 5960467 A	☐	Apparatus for efficiently providing memory operands for instructions	711/214
129	US 5958043 A	☐	Superscalar processor with forward map buffer in multiple instruction parallel issue/execution management system	712/216
130	US 5956495 A	☐	Method and system for processing branch instructions during emulation in a data processing system	703/26
131	US 5954815 A	☐	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
132	US 5953520 A	☐	Address translation buffer for data processing system emulation mode	703/26
133	US 5951679 A	☐	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
134	US 5951675 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/215
135	US 5951674 A	☐	Object-code compatible representation of very long instruction word programs	712/210

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136	US 5948060 A	☐	Speeding-up communication rates on links transferring data structures by a method of handing scatter/gather of storage blocks in commanded computer systems	709/212
137	US 5946705 A	☐	Avoidance of cache synonyms	711/108
138	US 5946468 A	☐	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
139	US 5944811 A	☐	Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies	712/23
140	US 5941984 A	☐	Data processing device	712/218
141	US 5941983 A	☐	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issurance of instructions from the queues	712/214
142	US 5933629 A	☐	Apparatus and method for detecting microbranches early	712/248
143	US 5933627 A	☐	Thread switch on blocked load or store using instruction thread field	712/228
144	US 5933626 A	☐	Apparatus and method for tracing microprocessor instructions	712/227
145	US 5933618 A	☐	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
146	US 5931957 A	☐	Support for out-of-order execution of loads and stores in a processor	714/48
147	US 5930520 A	☐	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	712/23
148	US 5928353 A	☐	Clear processing of a translation lookaside buffer with less waiting time	712/200
149	US 5926645 A	☐	Method and system for enabling multiple store instruction completions in a processing system	712/23
150	US 5925114 A	☐	Modem implemented in software for operation on a general purpose computer having operating system with different execution priority levels	710/48
151	US 5923862 A	☐	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
152	US 5920710 A	☐	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
153	US 5918062 A	☐	Microprocessor including an efficient implemention of an accumulate instruction	712/7
154	US 5918046 A	☐	Method and apparatus for a branch instruction pointer table	712/239
155	US 5915110 A	☐	Branch misprediction recovery in a reorder buffer having a future file	712/239
156	US 5913059 A	☐	Multi-processor system for inheriting contents of register from parent thread to child thread	718/104
157	US 5913050 A	☐	Method and apparatus for providing address-size backward compatibility in a processor using segmented memory	711/213
158	US 5913048 A	☐	Dispatching instructions in a processor supporting out-of-order execution	712/215

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159	US 5913047 A	☐	Pairing floating point exchange instruction with another floating point instruction to reduce dispatch latency	712/213
160	US 5909567 A	☐	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
161	US 5907860 A	☐	System and method of retiring store data from a write buffer	711/117
162	US 5907702 A	☐	Method and apparatus for decreasing thread switch latency in a multithread processor	718/108
163	US 5903918 A	☐	Program counter age bits	711/220
164	US 5903741 A	☐	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
165	US 5903740 A	☐	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
166	US 5901302 A	☐	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215
167	US 5900024 A	☐	Method for processing type-ahead input and operation-abort input	712/225
168	US 5898882 A	☐	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage	712/23
169	US 5898865 A	☐	Apparatus and method for predicting an end of loop for string instructions	712/239
170	US 5898864 A	☐	Method and system for executing a context-altering instruction without performing a context-synchronization operation within high-performance processors	712/228
171	US 5898852 A	☐	Load instruction steering in a dual data cache microarchitecture	712/214
172	US 5896518 A	☐	Instruction queue scanning using opcode identification	712/208
173	US 5894582 A	☐	Method of controlling parallel processing at an instruction level and processor for realizing the method	712/23
174	US 5894575 A	☐	Method and system for initial state determination for instruction trace reconstruction	717/128
175	US 5892936 A	☐	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
176	US 5889947 A	☐	Apparatus and method for executing instructions that select a storage location for output values in response to an operation count	709/213
177	US 5887174 A	☐	System, method, and program product for instruction scheduling in the presence of hardware lookahead accomplished by the rescheduling of idle slots	717/161
178	US 5887161 A	☐	Issuing instructions in a processor supporting out-of-order execution	712/244
179	US 5887152 A	☐	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
180	US 5884058 A	☐	Method for concurrently dispatching microcode and directly-decoded instructions in a microprocessor	712/214
181	US 5881307 A	☐	Deferred store data read with simple anti-dependency pipeline inter-lock control in superscalar processor	712/23

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182	US 5878244 A	☐	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
183	US 5878242 A	☐	Method and system for forwarding instructions in a processor with increased forwarding probability	712/216
184	US 5873115 A	☐	Cache memory	711/129
185	US 5872951 A	☐	Reorder buffer having a future file for storing speculative instruction execution results	712/218
186	US 5872949 A	☐	Apparatus and method for managing data flow dependencies arising from out-of-order execution, by an execution unit, of an instruction series input from an instruction source	712/216
187	US 5872946 A	☐	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
188	US 5870612 A	☐	Method and apparatus for condensed history buffer	710/260
189	US 5870579 A	☐	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
190	US 5870577 A	☐	System and method for dispatching two instructions to the same execution unit in a single cycle	712/215
191	US 5870575 A	☐	Indirect unconditional branches in data processing system emulation mode	712/209
192	US 5868545 A	☐	Automatic article feeding system	414/808
193	US 5867734 A	☐	Multiple-reader multiple-writer queue for a computer system	710/52
194	US 5867698 A	☐	Apparatus and method for accessing a branch target buffer	712/238
195	US 5867684 A	☐	Method and processor that permit concurrent execution of a store multiple instruction and a dependent instruction	712/218
196	US 5867682 A	☐	High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations	712/210
197	US 5867680 A	☐	Microprocessor configured to simultaneously dispatch microcode and directly-decoded instructions	712/204
198	US 5864690 A	☐	Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue	712/208
199	US 5864341 A	☐	Instruction dispatch unit and method for dynamically classifying and issuing instructions to execution units with non-uniform forwarding	712/214
200	US 5860014 A	☐	Method and apparatus for improved recovery of processor state using history buffer	710/260

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1	US 5860014 A	☐	Method and apparatus for improved recovery of processor state using history buffer	710/260
2	US 5859998 A	☐	Hierarchical microcode implementation of floating point instructions for a microprocessor	712/222
3	US 5859992 A	☐	Instruction alignment using a dispatch list and a latch list	712/204
4	US 5857097 A	☐	Method for identifying reasons for dynamic stall cycles during the execution of a program	712/236
5	US 5857089 A	☐	Floating point stack and exchange instruction	712/222
6	US 5850563 A	☐	Processor and method for out-of-order completion of floating-point operations during load/store multiple operations	712/23
7	US 5850542 A	☐	Microprocessor instruction hedge-fetching in a multiprediction branch environment	712/235
8	US 5845102 A	☐	Determining microcode entry points and prefix bytes using a parallel logic technique	712/211
9	US 5841999 A	☐	Information handling system having a register remap structure using a content addressable table	712/217
10	US 5838940 A	☐	Method and apparatus for rotating active instructions in a parallel data processor	712/216
11	US 5835968 A	☐	Apparatus for providing memory and register operands concurrently to functional units	711/214
12	US 5832292 A	☐	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
13	US 5829021 A	☐	System for controlling operating timing of a cache memory	711/118
14	US 5828873 A	☐	Assembly queue for a floating point unit	712/222
15	US 5828868 A	☐	Processor having execution core sections operating at different clock rates	713/501
16	US 5826096 A	☐	Minimal instruction set computer architecture and multiple instruction issue method	712/24
17	US 5826073 A	☐	Self-modifying code handling system	712/226
18	US 5826055 A	☐	System and method for retiring instructions in a superscalar microprocessor	712/218
19	US 5826053 A	☐	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
20	US 5822603 A	☐	High bandwidth media processor interface for transmitting data in the form of packets with requests linked to associated responses by identification data	712/1
21	US 5822574 A	☐	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
22	US 5822570 A	☐	System and method for parsing and executing a single instruction stream using a plurality of tightly coupled parsing and execution units	703/26
23	US 5822556 A	☐	Distributed completion control in a microprocessor	712/205

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24	US 5819114 A	☐	Interrupption recovery and resynchronization of events in a computer	710/57
25	US 5813039 A	☐	Guest execution control system, method and computer process for a virtual machine system	711/156
26	US 5812811 A	☐	Executing speculative parallel instructions threads with forking and inter-thread communication	712/216
27	US 5809324 A	☐	Multiple instruction dispatch system for pipelined microprocessor without branch breaks	712/23
28	US 5809321 A	☐	General purpose, multiple precision parallel operation, programmable media processor	712/1
29	US 5809320 A	☐	High-performance multi-processor having floating point unit	712/34
30	US 5809276 A	☐	System and method for register renaming	712/217
31	US 5809268 A	☐	Method and system for tracking resource allocation within a processor	712/200
32	US 5805916 A	☐	Method and apparatus for dynamic allocation of registers for intermediate floating-point results	712/23
33	US 5805906 A	☐	Method and apparatus for writing information to registers in a data processing system using a number of registers for processing instructions	710/260
34	US 5802556 A	☐	Method and apparatus for correcting misaligned instruction data	711/109
35	US 5796996 A	☐	Processor apparatus and its control method for controlling a processor having a CPU for executing an instruction according to a control program	712/225
36	US 5794061 A	☐	General purpose, multiple precision parallel operation, programmable media processor	712/1
37	US 5794060 A	☐	General purpose, multiple precision parallel operation, programmable media processor	712/1
38	US 5787303 A	☐	Digital computer system capable of processing a plurality of instructions in parallel based on a VLIW architecture	712/24
39	US 5784324 A	☐	Single-chip memory system having a multiple bit line structure for outputting a plurality of data simultaneously	365/207
40	US 5778221 A	☐	System for executing asynchronous branch and link in parallel processor	712/244
41	US 5771366 A	☐	Method and system for interchanging operands during complex instruction execution in a data processing system	712/217
42	US 5768576 A	☐	Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor	712/238
43	US 5765221 A	☐	Method and system of addressing which minimize memory utilized to store logical addresses by storing high order bits within a register	711/220
44	US 5765220 A	☐	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
45	US 5765215 A	☐	Method and system for efficient rename buffer deallocation within a processor	711/214
46	US 5765016 A	☐	Reorder buffer configured to store both speculative and committed register states	712/23

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47	US 5764970 A	☐	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
48	US 5764938 A	☐	Resynchronization of a superscalar processor	712/200
49	US 5761473 A	☐	Method and system for increased instruction synchronization efficiency in a superscalar processsor system utilizing partial data dependency interlocking	712/217
50	US 5754813 A	☐	Data processor	712/216
51	US 5754811 A	☐	Instruction dispatch queue for improved instruction cache to queue timing	712/214
52	US 5751995 A	☐	Apparatus and method of maintaining processor ordering in a multiprocessor system which includes one or more processors that execute instructions speculatively	711/145
53	US 5751981 A	☐	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
54	US 5748978 A	☐	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
55	US 5742840 A	☐	General purpose, multiple precision parallel operation, programmable media processor	712/210
56	US 5742791 A	☐	Apparatus for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
57	US 5742784 A	☐	System for reordering of instructions before placement into cache to reduce dispatch latency	712/213
58	US 5742781 A	☐	Decoded instruction buffer apparatus and method for reducing power consumption in a digital signal processor	712/208
59	US 5740415 A	☐	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
60	US 5727177 A	☐	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
61	US 5724565 A	☐	Method and system for processing first and second sets of instructions by first and second types of processing systems	712/245
62	US 5721857 A	☐	Method and apparatus for saving the effective address of floating point memory operations in an out-of-order microprocessor	712/23
63	US 5706290 A	☐	Method and apparatus including system architecture for multimedia communication	370/465
64	US 5699537 A	☐	Processor microarchitecture for efficient dynamic scheduling and execution of chains of dependent instructions	712/217
65	US 5699536 A	☐	Computer processing system employing dynamic instruction formatting	712/216
66	US 5696955 A	☐	Floating point stack and exchange instruction	712/222
67	US 5696939 A	☐	Apparatus and method using a semaphore buffer for semaphore instructions	711/150
68	US 5694565 A	☐	Method and device for early deallocation of resources during load/store multiple operations to allow simultaneous dispatch/execution of subsequent instructions	712/216
69	US 5692170 A	☐	Apparatus for detecting and executing traps in a superscalar processor	712/244

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70	US 5689720 A	☐	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
71	US 5682521 A	☐	Microprocessor control system which selects operating instructions and operands in an order based upon the number of transferred executable operating instructions	712/200
72	US 5680597 A	☐	System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions	712/226
73	US 5675776 A	☐	Data processor using FIFO memories for routing operations to parallel operational units	712/220
74	US 5664215 A	☐	Data processor with an execution unit for performing load instructions and method of operation	712/23
75	US 5664136 A	☐	High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations	712/208
76	US 5664120 A	☐	Method for executing instructions and execution unit instruction reservation table within an in-order completion processor	712/217
77	US 5659782 A	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/23
78	US 5655098 A	☐	High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format	712/210
79	US 5655097 A	☐	High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format	712/204
80	US 5651125 A	☐	High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
81	US 5649232 A	☐	Structure and method for multiple-level read buffer supporting optimal throttled read operations by regulating transfer rate	710/60
82	US 5649225 A	☐	Resynchronization of a superscalar processor	712/23
83	US 5649137 A	☐	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
84	US 5636363 A	☐	Hardware control structure and method for off-chip monitoring entries of an on-chip cache	711/138
85	US 5634136 A	☐	Data processor and method of controlling the same	712/237
86	US 5633813 A	☐	Apparatus and method for automatic test generation and fault simulation of electronic circuits, based on programmable logic circuits	703/14
87	US 5630082 A	☐	Apparatus and method for instruction queue scanning	712/213
88	US 5625785 A	☐	Information processing apparatus having dual buffers for transmitting debug data to an external debug unit	712/227
89	US 5623615 A	☐	Circuit and method for reducing prefetch cycles on microprocessors	712/238
90	US 5618096 A	☐	Data processor with unified store queue permitting hit under miss memory accesses	711/118
91	US 5619730 A	☐	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	710/35

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92	US 5619679 A	☐	Memory control device and method operated in consecutive access mode	711/167
93	US 5619667 A	☐	Method and apparatus for fast fill of translator instruction queue	712/208
94	US 5613080 A	☐	Multiple execution unit dispatch with instruction shifting between first and second instruction buffers based upon data dependency	712/214
95	US 5611063 A	☐	Method for executing speculative load instructions in high-performance processors	712/205
96	US 5606675 A	☐	Data processor for invalidating prefetched instruction or branch history information	712/237
97	US 5604909 A	☐	Apparatus for processing instructions in a computing system	712/208
98	US 5604877 A	☐	Method and apparatus for resolving return from subroutine instructions in a computer processor	712/243
99	US 5594864 A	☐	Method and apparatus for unobtrusively monitoring processor states and characterizing bottlenecks in a pipelined processor executing grouped instructions	714/39
100	US 5592679 A	☐	Apparatus and method for distributed control in a processor architecture	712/23
101	US 5592634 A	☐	Zero-cycle multi-state branch cache prediction data processing system and method thereof	712/239
102	US 5590295 A	☐	System and method for register renaming	712/217
103	US 5586295 A	☐	Combination prefetch buffer and instruction cache	711/137
104	US 5584037 A	☐	Entry allocation in a circular buffer	712/23
105	US 5581775 A	☐	History buffer system	712/240
106	US 5574939 A	☐	Multiprocessor coupling system with integrated compile and run time scheduling for parallelism	712/24
107	US 5564041 A	☐	Microprocessor for inserting a bus cycle in an instruction set to output an internal information for an emulation	703/23
108	US 5561761 A	☐	Central processing unit data entering and interrogating device and method therefor	714/30
109	US 5560032 A	☐	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
110	US 5557763 A	☐	System for handling load and/or store operations in a superscalar microprocessor	712/23
111	US 5553254 A	☐	Instruction cache access and prefetch process controlled by a predicted instruction-path mechanism	712/207
112	US 5542058 A	☐	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
113	US 5539911 A	☐	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
114	US 5537559 A	☐	Exception handling circuit and method	712/244

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115	US 5537553 A	☐	Method of and apparatus for bus control and data processor	710/100
116	US 5535410 A	☐	Parallel processor having decoder for selecting switch from the group of switches and concurrently inputting MIMD instructions while performing SIMD operation	712/20
117	US 5530889 A	☐	Hierarchical structure processor having at least one sub-sequencer for executing basic instructions of a macro instruction	712/247
118	US 5524255 A	☐	Method and apparatus for accessing global registers in a multiprocessor system	712/203
119	US 5524221 A	☐	Next instruction pointer calculation system for a microcomputer	712/230
120	US 5517639 A	☐	System for outputting execution time of industrial automated apparatus	700/108
121	US 5511175 A	☐	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
122	US 5511172 A	☐	Speculative execution processor	712/235
123	US 5509130 A	☐	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
124	US 5503516 A	☐	Automatic article feeding system	414/800
125	US 5500943 A	☐	Data processor with rename buffer and FIFO buffer for in-order instruction completion	712/218
126	US 5491829 A	☐	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system	712/23
127	US 5488730 A	☐	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
128	US 5481743 A	☐	Minimal instruction set computer architecture and multiple instruction issue method	712/23
129	US 5481689 A	☐	Conversion of internal processor register commands to I/O space addresses	711/202
130	US 5471591 A	☐	Combined write-operand queue and read-after-write dependency scoreboard	712/217
131	US 5465373 A	☐	Method and system for single cycle dispatch of multiple instructions in a superscalar processor system	712/215
132	US 5465372 A	☐	Dataflow computer for following data dependent path processes	712/25
133	US 5452427 A	☐	Data processing device for variable word length instruction system having short instruction execution time and small occupancy area	712/210
134	US 5450555 A	☐	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
135	US 5438670 A	☐	Method of prechecking the validity of a write access request	711/3
136	US 5437017 A	☐	Method and system for maintaining translation lookaside buffer coherency in a multiprocessor data processing system	709/213
137	US 5434985 A	☐	Simultaneous prediction of multiple branches for superscalar processing	712/240

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138	US 5418973 A	☐	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
139	US 5414822 A	☐	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
140	US 5404471 A	☐	Method and apparatus for switching address generation modes in CPU having plural address generation modes	712/207
141	US 5394529 A	☐	Branch prediction unit for high-performance processor	712/240
142	US 5392391 A	☐	High performance graphics applications controller	345/503
143	US 5381532 A	☐	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
144	US 5381531 A	☐	Data processor for selective simultaneous execution of a delay slot instruction and a second subsequent instruction the pair following a conditional branch instruction	712/235
145	US 5380138 A	☐	Automatic article feeding system	414/277
146	US 5349656 A	☐	Task scheduling method in a multiprocessor system where task selection is determined by processor identification and evaluation information	718/102
147	US 5335330 A	☐	Information processing apparatus with optimization programming	712/241
148	US 5332996 A	☐	Combined queue for invalidates and return data in multiprocessor system	711/171
149	US 5317720 A	☐	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
150	US 5317711 A	☐	Structure and method for monitoring an internal cache	714/47
151	US 5313602 A	☐	Multiprocessor system and method of control over order of transfer of data between buffer storages	711/100
152	US 5305458 A	☐	Multiple virtual storage system and address control apparatus having a designation table holding device and translation buffer	711/207
153	US 5299318 A	☐	Processor with a plurality of microprogrammed units, with anticipated execution indicators and means for executing instructions in pipeline manner	712/231
154	US 5293602 A	☐	Multiprocessor computer system with dedicated synchronizing cache	711/147
155	US 5287466 A	☐	Method and apparatus for parallel loads equalizing utilizing instruction sorting by columns based on predicted instruction execution time	712/206
156	US 5267350 A	☐	Method for fetching plural instructions using single fetch request in accordance with empty state of instruction buffers and setting of flag latches	712/205
157	US 5265213 A	☐	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
158	US 5251306 A	☐	Apparatus for controlling execution of a program in a computing device	712/217
159	US 5241644 A	☐	Queue having long word length	710/54
160	US 5233696 A	☐	Microprocessor having precoder unit and main decoder unit operating in pipeline processing manner	712/204

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161	US 5232331 A	☐	Automatic article feeding system	414/802
162	US 5226132 A	☐	Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (STO) while using space registers as storage devices for a data processing system	711/209
163	US 5218678 A	☐	System and method for atomic access to an input/output device with direct memory access	710/5
164	US 5202967 A	☐	Data processing apparatus for performing parallel decoding and parallel execution of a variable word length instruction	712/212
165	US 5201057 A	☐	System for extracting low level concurrency from serial instruction streams	712/18
166	US 5197145 A	☐	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143
167	US 5197131 A	☐	Instruction buffer system for switching execution of current instruction to a branch or to a return from subroutine	712/238
168	US 5185871 A	☐	Coordination of out-of-sequence fetching between multiple processors using re-execution of instructions	712/205
169	US 5185868 A	☐	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
170	US 5179530 A	☐	Architecture for integrated concurrent vector signal processor	708/520
171	US 5163139 A	☐	Instruction preprocessor for conditionally combining short memory instructions into virtual long instructions	712/206
172	US 5157388 A	☐	Method and apparatus for graphics data interpolation	345/673
173	US 5155843 A	☐	Error transition mode for multi-processor system	714/5
174	US 5142631 A	☐	System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register	712/217
175	US 5131086 A	☐	Method and system for executing pipelined three operand construct	712/213
176	US 5125079 A	☐	Method for controlling the data transmission of a central unit interfacing control circuit and circuit arrangement for the implementation of the method	710/305
177	US 5115496 A	☐	Queue device capable of quickly transferring a digital signal unit of a word length different from a single word length	711/212
178	US 5101346 A	☐	Virtual machine system having a plurality of real instruction processors and virtual machines, and a registration table	718/100
179	US 5101341 A	☐	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
180	US 5081698 A	☐	Method and apparatus for graphics display data manipulation	345/422
181	US 5050076 A	☐	Prefetching queue control system	712/219
182	US RE33629 E	☐	Numeric data processor	708/510

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183	US 5029080 A	☐	Method and apparatus for composing a set of instructions for executing a data flow program defined by structured data	712/201
184	US 5018145 A	☐	IC tester	714/743
185	US 4992938 A	☐	Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers	712/217
186	US 4974198 A	☐	Vector processing system utilizing firm ware control to prevent delays during processing operations	712/8
187	US 4974154 A	☐	Computer with instruction prefetch queue retreat unit	712/240
188	US 4953225 A	☐	Handwritten character-recognizing apparatus for automatically generating and displaying character frames	382/179
189	US 4953121 A	☐	Circuitry for and method of controlling an instruction buffer in a data-processing system	712/241
190	US 4910657 A	☐	Microprocessor providing bus access for unconditional instruction execution	712/207
191	US 4893233 A	☐	Method and apparatus for dynamically controlling each stage of a multi-stage pipelined data unit	712/244
192	US 4858105 A	☐	Pipelined data processor capable of decoding and executing plural instructions in parallel	712/235
193	US 4858104 A	☐	Preceding instruction address based branch prediction in a pipelined processor	712/240
194	US 4847753 A	☐	Pipelined computer	712/238
195	US 4847748 A	☐	Virtual memory arrangement data processing system with decoding and execution of prefetched instructions in parallel	712/212
196	US 4831515 A	☐	Information processing apparatus for determining sequence of parallel executing instructions in response to storage requirements thereof	712/217
197	US 4766566 A	☐	Performance enhancement scheme for a RISC type VLSI processor using dual execution units for parallel instruction processing	712/23
198	US 4761731 A	☐	Look-ahead instruction fetch control for a cache memory	711/156
199	US 4758949 A	☐	Information processing apparatus	712/208
200	US 4742453 A	☐	Pipeline-controlled information processing system for generating updated condition code	712/234